**Nano III**

# Micro- and nano-fabrication

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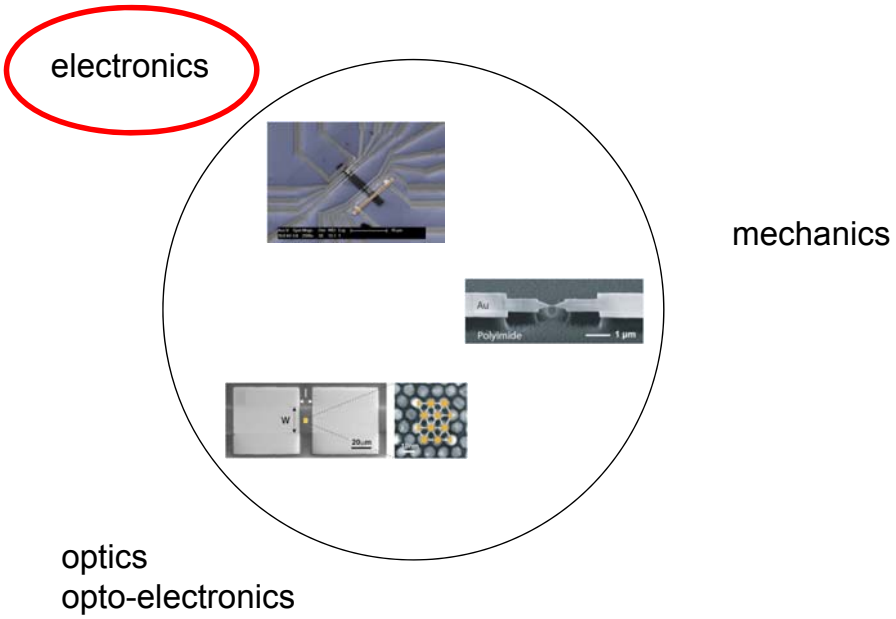
## nanofabrication: tools for nanoscale devices




NB: needs for research ≠ needs for industrial production

# Outline

- Introduction:
  **overview, state of the art**
  **a bit of semiconductor physics** (⇨ CMOS)

- Fabrication basics
  - **IC fabrication overview**
  - clean-rooms
  - Silicon: from sand to wafer
  - **material deposition techniques**
  - **etching**
  - **lithography**
  - **examples** of devices: MEMS, NEMS

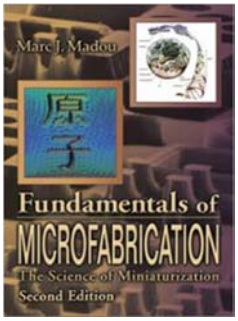
- Outlook: new and future techniques



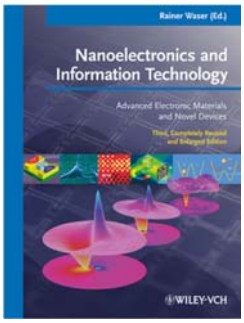
# References

**overview books**

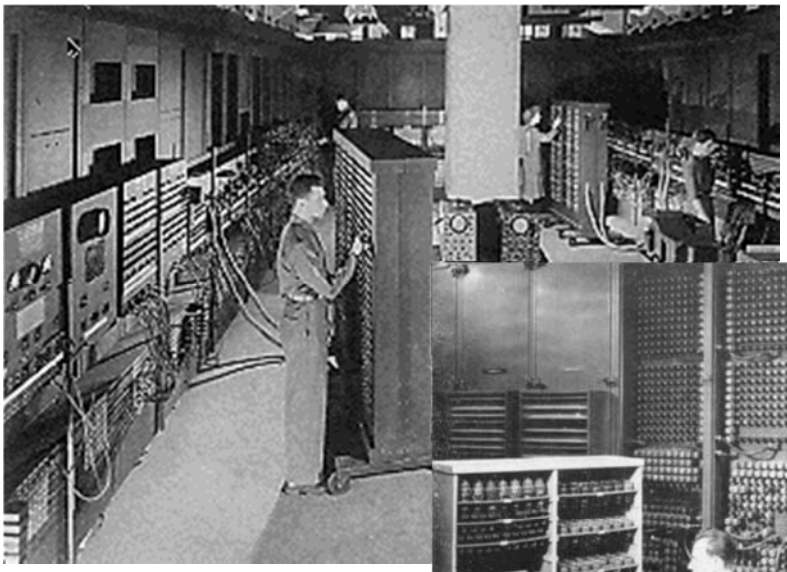
- **Fundamentals of Microfabrication: The Science of Miniaturization** M. Madou, 2nd ed., CRC Press, 2002

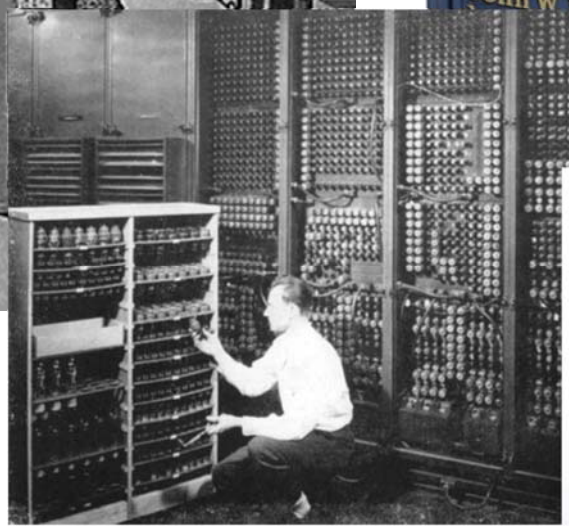



- **Nanoelectronics and Information Technology** R. Waser ed., Wiley-VCH, 2012



# Introduction



*http://ei.cs.vt.edu/~history/ENIAC.Richey.HTML*

**ENIAC, 1946**
*(18,000 vacuum tubes)*

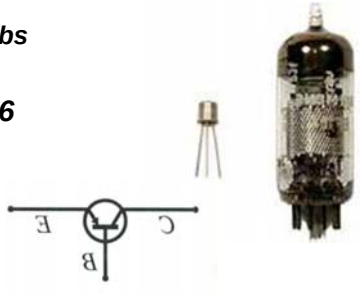


# Introduction

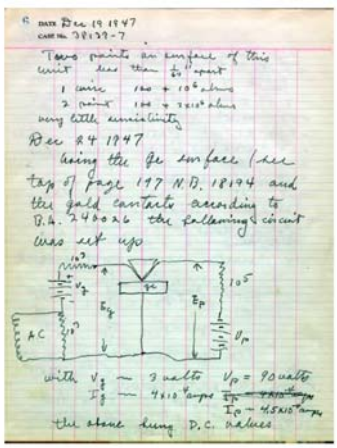
**1947, 24th December**
***John Bardeen***
***Walter Brattain***
***William Schockley***

***ATT Bell Labs***

***Nobel 1956***

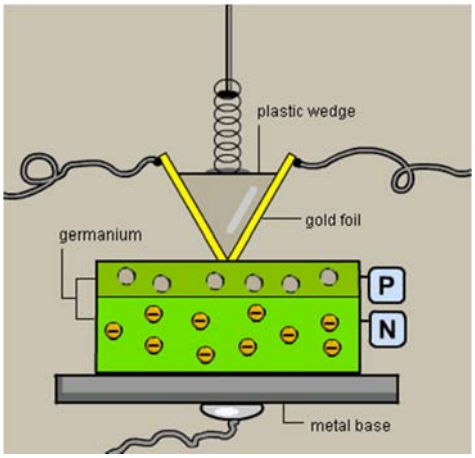



**first point contact transfer resistor**



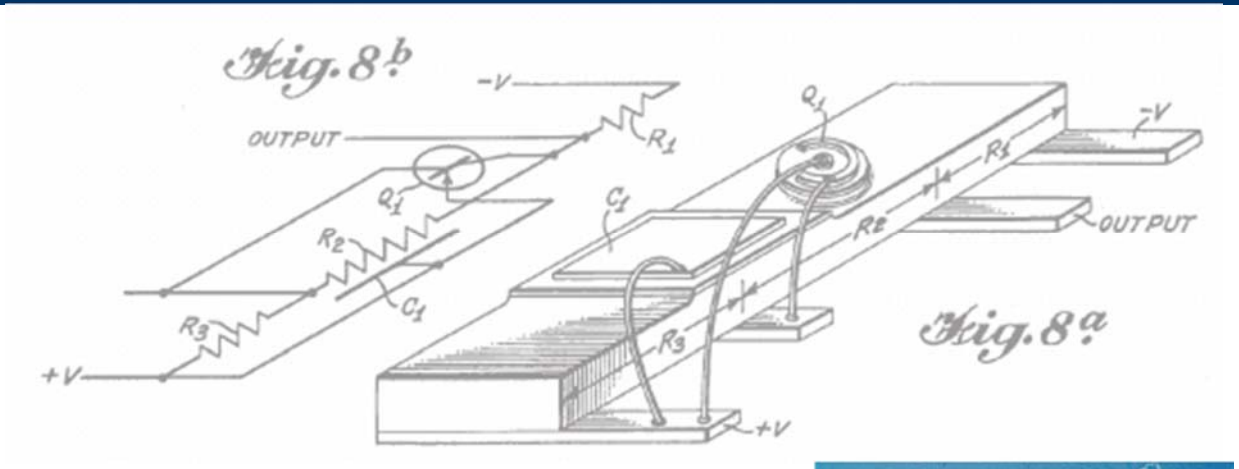
***Bell labs***

***Bell labs***




***nobel.se***

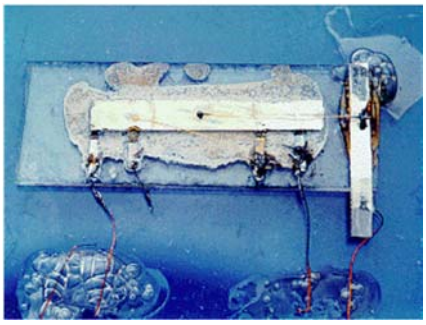
# Introduction




**1958**

**Jack Kilby, Texas Instruments**

**first IC (Integrated Circuit)**



***Nobel in 2000 (for the IC)***

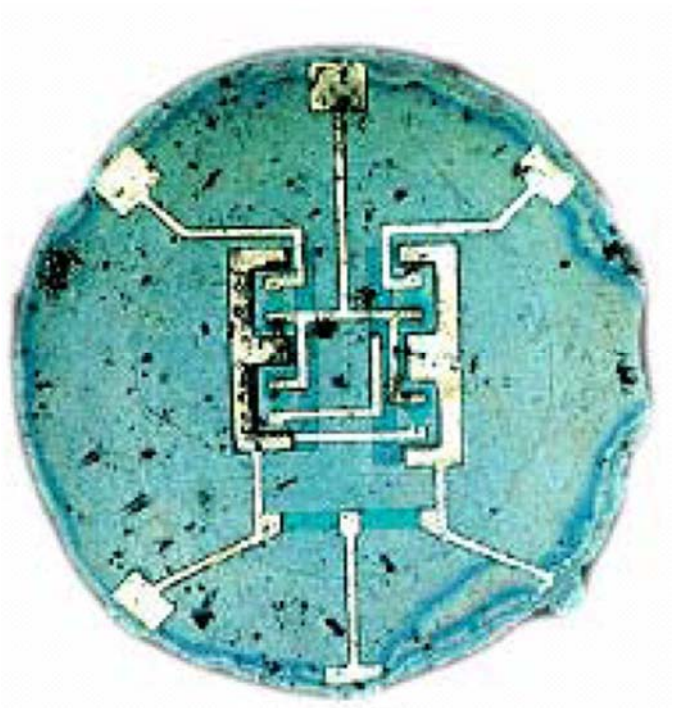
*together with Alferov & Krömer (for work on information and communication technology)*



# Introduction

**1961, Robert Noyce, Fairchild Camera**

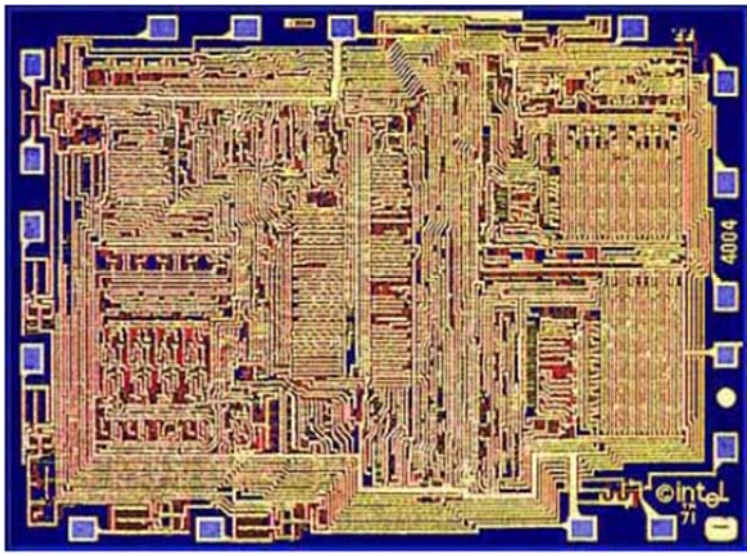
**first integrated circuit available as a monolithic chip**



***Planar technology***

***(Si substrate and Al lines)***

# Introduction




**1971** **Intel anounces the i4004 microprocessor**
**"a new era of integrated electronics"**
**2250 transistors, 10μm technology, 108kHz**

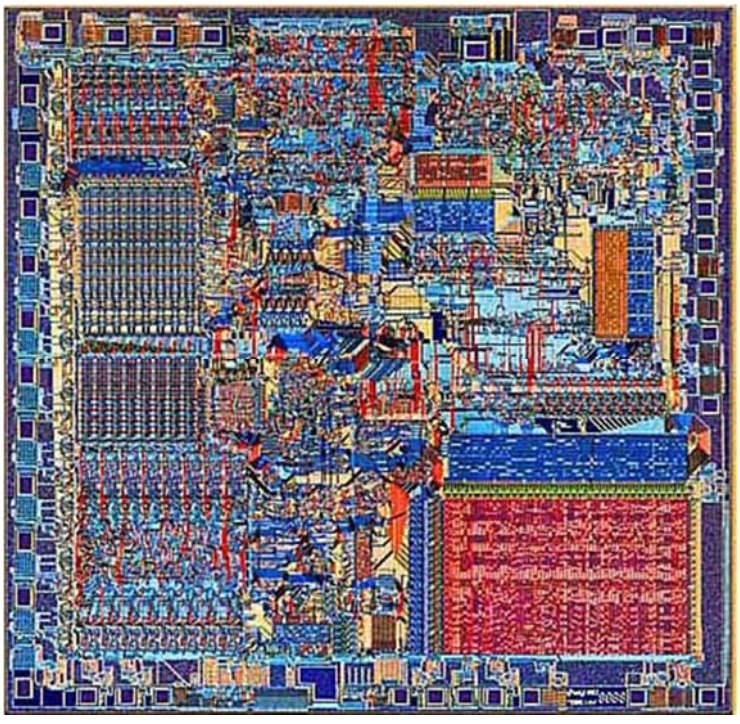


http://www.intel.com

# Introduction

**1981**
**Intel i8088**
**29000 transistors, 3μm technology, 8MHz**

**invention of the PC (personal computer)**
**IBM, A.Child, B.Gates**

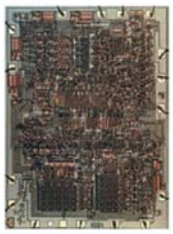




http://www.intel.com

# Introduction

1971

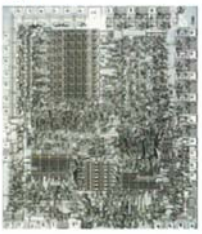


**Intel® 4004 processor**
Initial clock speed: 108KHz
Transistors: 2,300
Manufacturing technology:
10 micron

1972

**Intel® 8008 processor**
Initial clock speed: 800KHz
Transistors: 3,500
Manufacturing technology:
10 micron

1974

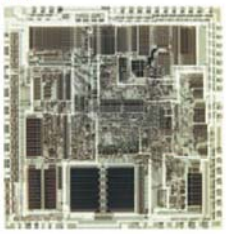


**Intel® 8080 processor**
Initial clock speed: 2MHz
Transistors: 4,500
Manufacturing technology:
6 micron

1978

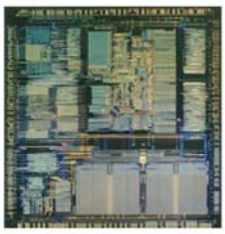
**Intel® 8086 processor**
Initial clock speed: 5MHz
Transistors: 29,000
Manufacturing technology:
3 micron

1982



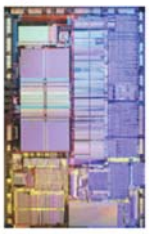
**Intel® 286 processor**
Initial clock speed: 6MHz
Transistors: 134,000
Manufacturing technology:
1.5 micron

1985



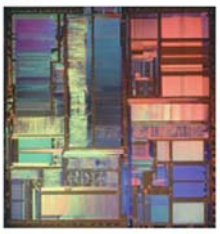
**Intel386™ processor**
Initial clock speed: 16MHz
Transistors: 275,000
Manufacturing technology:
1.5 micron

1989



**Intel486™ processor**
Initial clock speed: 25MHz
Transistors: 1.2 million
Manufacturing technology:
1 micron

1993



**Intel® Pentium® processor**
Initial clock speed: 66MHz
Transistors: 3.1 million
Manufacturing technology:
0.8 micron

1995

**Intel® Pentium® Pro processor**
Initial clock speed: 200MHz
Transistors: 5.5 million
Manufacturing technology:
0.35 micron



***http://www.intel.com***

# Introduction

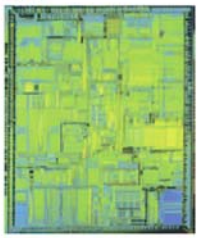
1997

**Intel® Pentium® II processor**
Initial clock speed: 300MHz
Transistors: 7.5 million
Manufacturing technology:
0.25 micron

1998

**Intel® Celeron® processor**
Initial clock speed: 266MHz
Transistors: 7.5 million
Manufacturing technology:
0.25 micron

1999



**Intel® Pentium® III processor**
Initial clock speed: 600MHz
Transistors: 9.5 million
Manufacturing technology:
0.25 micron

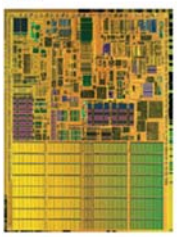
2000

**Intel® Pentium® 4 processor**
Initial clock speed: 1.5GHz
Transistors: 42 million
Manufacturing technology:
0.18 micron

2001

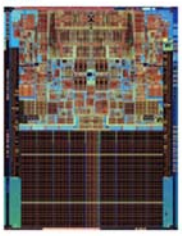
**Intel® Xeon® processor**
Initial clock speed: 1.7GHz
Transistors: 42 million
Manufacturing technology:
0.18 micron

2003



**Intel® Pentium® M processor**
Initial clock speed: 1.7GHz
Transistors: 55 million
Manufacturing technology:
90nm

2006



**Intel® Core™2 Duo processor**
Initial clock speed: 2.66GHz
Transistors: 291 million
Manufacturing technology:
65nm

2008

**Intel® Core™2 Duo processor**
Initial clock speed: 2.4GHz
Transistors: 410 million
Manufacturing technology:
45nm

2008

**Intel® Atom™ processor**
Initial clock speed: 1.86GHz
Transistors: 47 million
Manufacturing technology:
45nm

2010

**2nd generation**
**Intel® Core™ processor**
Initial clock speed: 3.8GHz
Transistors: 1.16 billion
Manufacturing technology:
32nm

2012

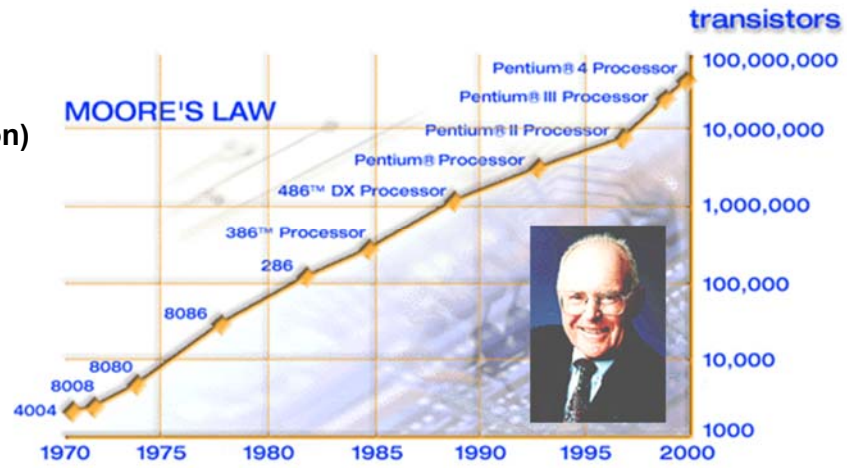
**3rd generation**
**Intel® Core™ processor**
Initial clock speed: 2.9GHz
Transistors: 1.4 billion
Manufacturing technology:
22nm



***http://www.intel.com***

# Introduction

1965, **Gordon E. Moore**
**(co-founder Intel Corporation)**




*Electronics, Vol. 38(8), 1965*

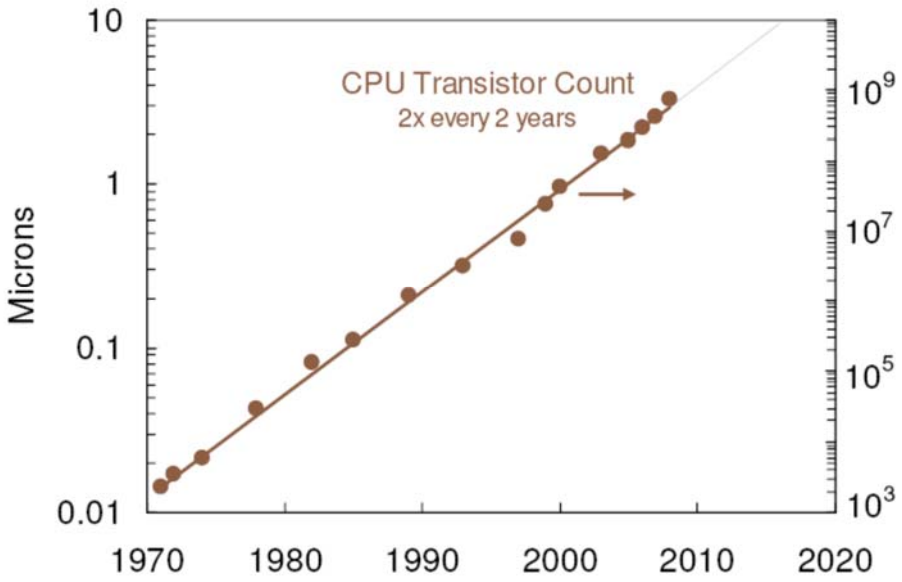
"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short this rate can be expected to continue, if not increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years."



http://www.pbs.org/transistor/

# Introduction

**Scaling trends**

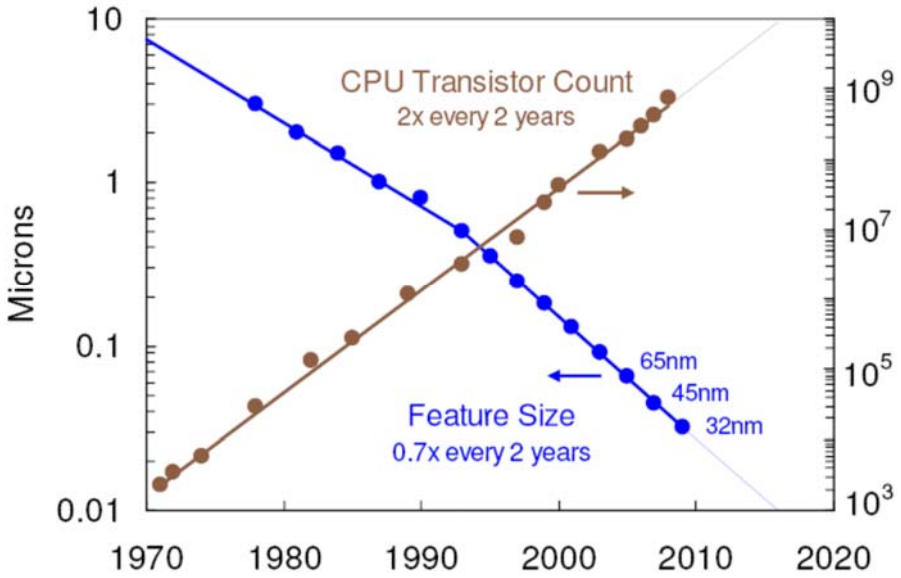





*M. Bohr, Intel*

# Introduction

## Scaling trends




**trend**
14nm (2014)
10nm (2016)

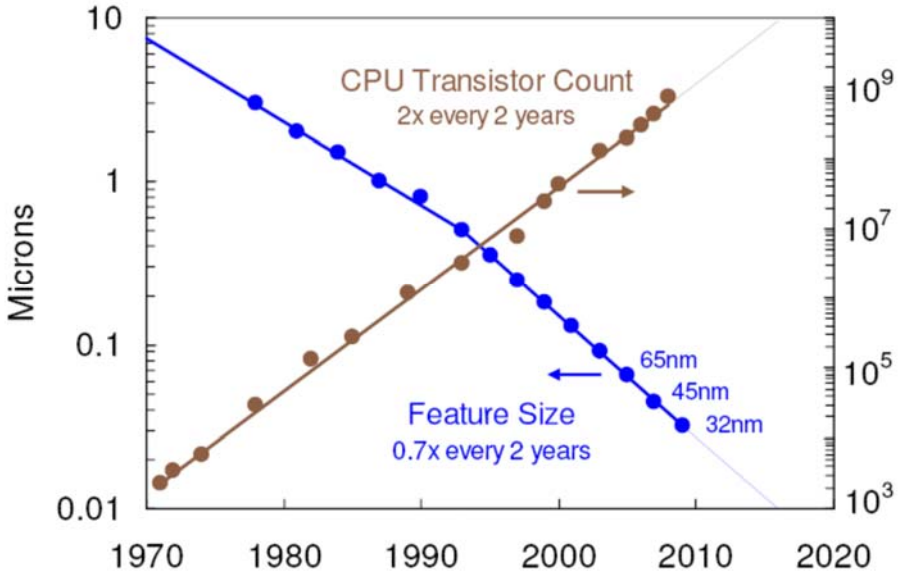
**performance ↗, power ↘, cost ↘** ***gate delay reduces by 30%, energy per logic operation reduces by 65%, & power consumption reduces by 50% (Borkar, IEEE Micro, 1999)***



***M. Bohr, Intel***

# Introduction

## Scaling trends




**trend**
14nm (2014)
10nm (2016)

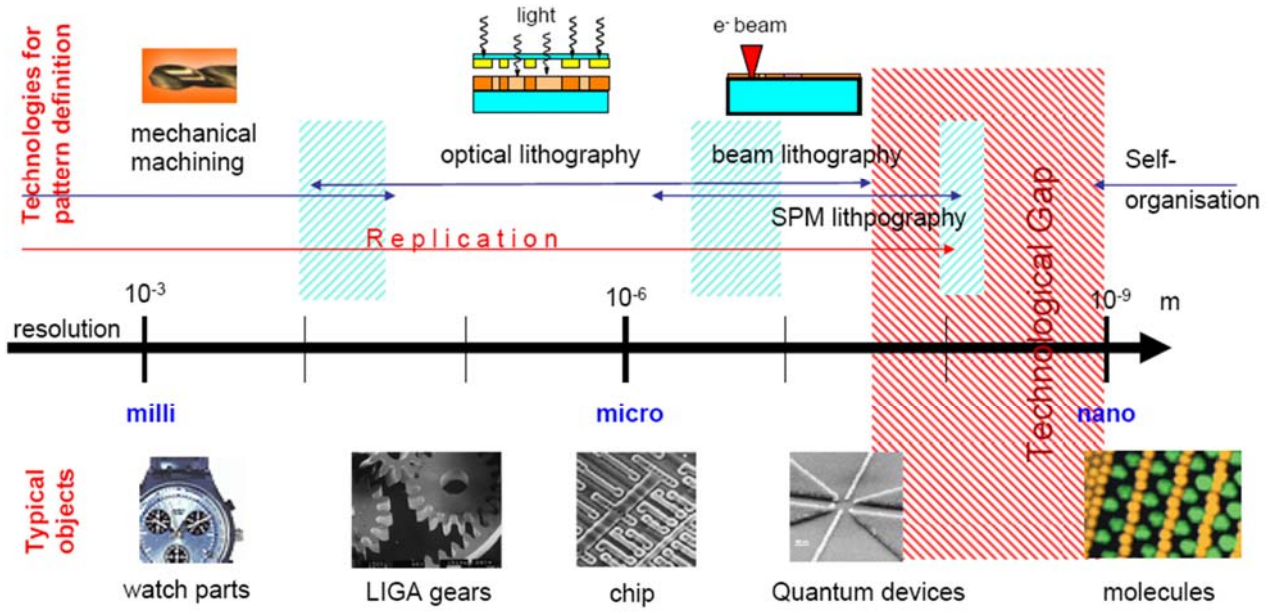
**density** ~$10^9$ transistors/5cm$^2$
A(transistor) ~ (700nm)$^2$

**scaling** A(chip) ⇨ A(soccer field, 50mx100m)
A(transistor) ~ (2mm)$^2$



***M. Bohr, Intel***

# Introduction






**J. Gobrecht, PSI**

# Introduction

top-down approach:

- extend current techniques to smaller sizes
- (EUV-L, x-ray lithography., nano-imprint, flip-up principle, i.e.: horizontal/vertical exchange, etc…)
- problem: precision, costs

bottom-up approach:

- start from individual atoms/molecules
- use principles of self-organization (self-assembly; inspiration from biology, biochemistry, chemistry)
- problem: long-range order difficult to achieve

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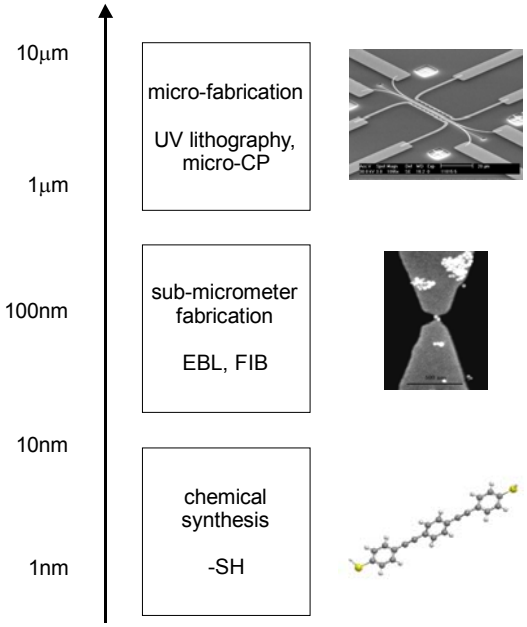


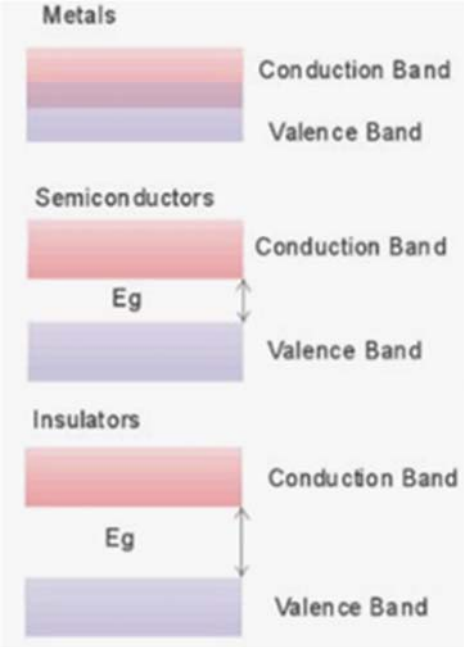

**nanofabrication (<100nm)** ⇔ combination of both routes

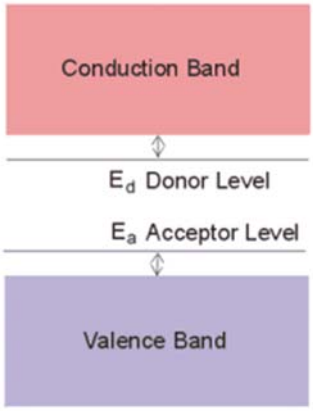


# Outline

- Introduction:
  - overview, state of the art,
  - a bit of semiconductor physics
  - (⇔ condensed matter course)
- Fabrication basics
  - IC fabrication overview
  - clean-rooms
  - Silicon: from sand to wafer
  - material deposition techniques
  - etching
  - lithography
  - examples of devices: MEMS, NEMS
- Outlook: new and future techniques

# Semiconductors physics reminder



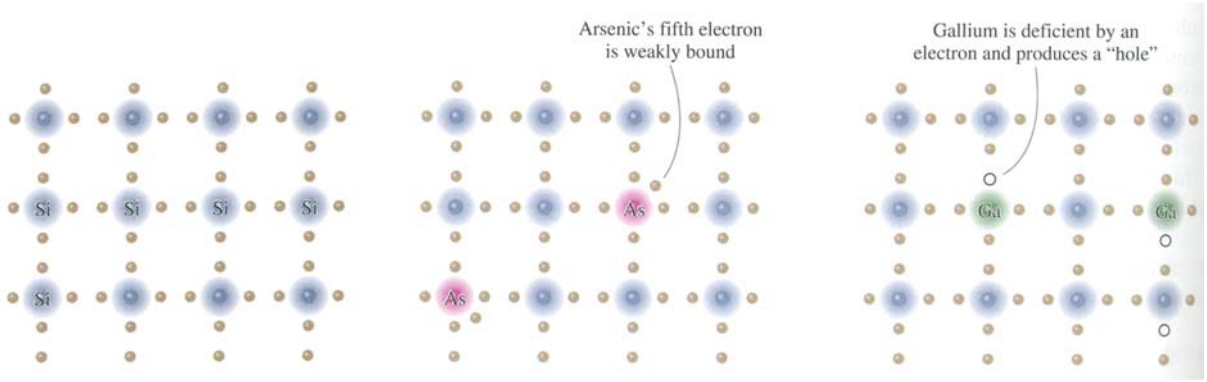

**Energy gaps**

Si ~ 1.12 eV
Ge ~ 0.66 eV
GaAs ~ 1.43 eV

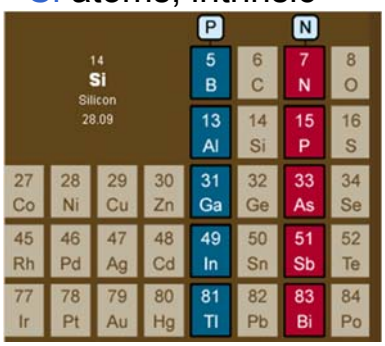
NB: kT (RT) ~25meV



# Semiconductors physics reminder




Si atoms, intrinsic



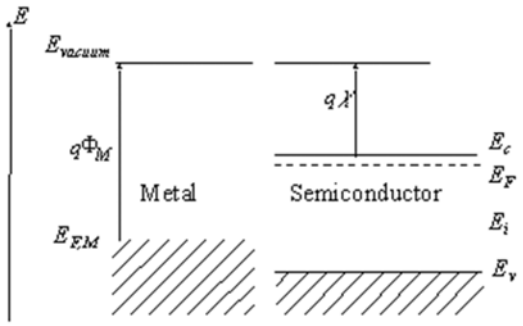

As doped Si
n-type
other donors:
P, Sb

Ga doped Si
p-type
other acceptors:
B, Al

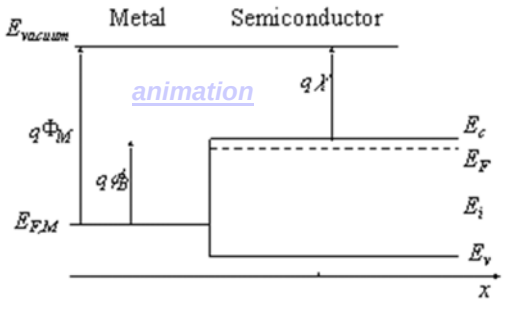
➔ e.g.: resistivity changes by > 6 orders of mag. with a 1ppm B doping

# Semiconductors physics reminder

**Energy band diagram** of a metal and a semiconductor



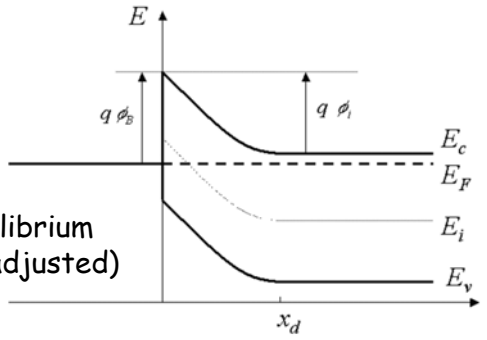

**before contact**




**after contact**

$\phi_B = \Phi_M - \chi$ , for an n-type semiconductor

$\phi_B = \frac{E_g}{q} + \chi - \Phi_M$ , for a p-type semiconductor




thermal equilibrium
(Fermi levels adjusted)



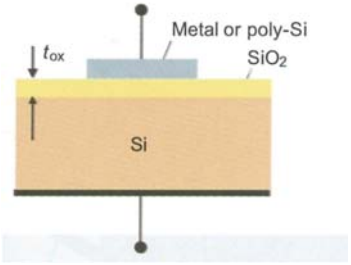
# Semiconductors physics reminder

**Workfunction** of selected metals and their measured barrier height (eV) on germanium, silicon and gallium arsenide.

| | Ag | Al | Au | Cr | Ni | Pt | W |
|---|---|---|---|---|---|---|---|
| **$\Phi_M$ (in vacuum)** | 4.3 | 4.25 | 4.8 | 4.5 | 4.5 | 5.3 | 4.6 |
| **n-Ge** | 0.54 | 0.48 | 0.59 | | 0.49 | | 0.48 |
| **p-Ge** | 0.5 | | 0.3 | | | | |
| **n-Si** | 0.78 | 0.72 | 0.8 | 0.61 | 0.61 | 0.9 | 0.67 |
| **p-Si** | 0.54 | 0.58 | 0.34 | 0.5 | 0.51 | | 0.45 |
| **n-GaAs** | 0.88 | 0.8 | 0.9 | | | 0.84 | 0.8 |
| **p-GaAs** | 0.63 | | 0.42 | | | | |

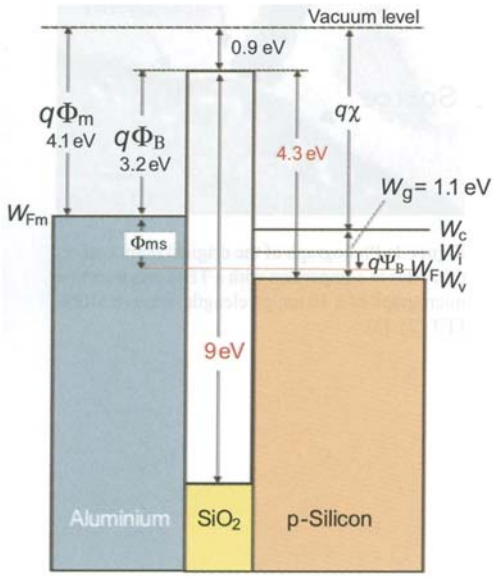
# Semiconductors physics reminder

## **MOSFET** technology: MOS capacitor




| | |
|---|---|
| Metal (gate) : | Al (Mo, W, Cu), Poly-Si |
| Oxide : | $SiO_2$, d ≈ 1.7-10 nm |
| Semiconductor : | p- or n-type silicon |
| doping | $10^{13}$ - $10^{18}$ $cm^{-3}$ |
| orientation typ. | <100> |

energy band diagram
Al/$SiO_2$/p-Si

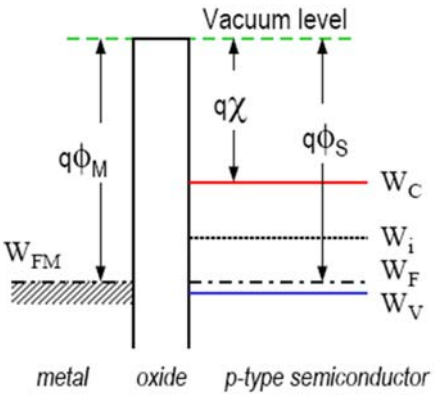





Ref. 3

# Semiconductors physics reminder

## MOS capacitor: ideal case




Energy band diagram of an ideal MOS structure
$q\phi_M$ = metal workfunction (Al: 4.1 eV)
$q\chi$ = semiconductor electron affinity (~ 4.05 eV)
$q\phi_S$ = semiconductor work function

**Assumptions for the ideal MOS structure:**
1. No workfunction difference between metal and semiconductor (aligned vacuum and Fermi niveaus)
2. charges at any bias exist only in the semiconductor and at the metal surface
3. no carrier transport through the oxide under dc-biasing conditions

i.e. **Flat band condition at V=0**
(potential **V** between gate and back contact)



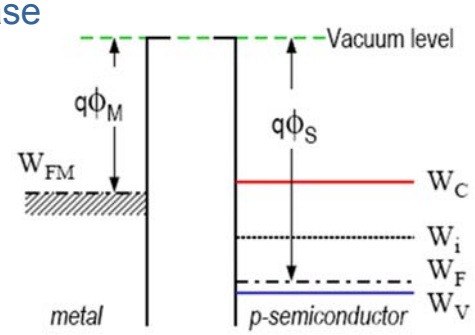
B. Föste, Infineon

# Semiconductors physics reminder

## MOS capacitor: real case

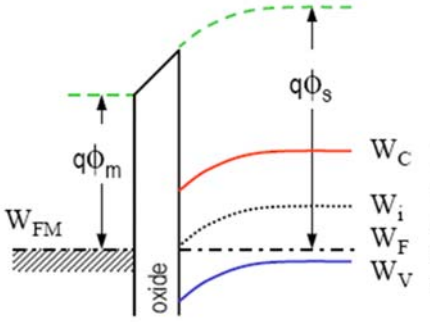
**Real MOS structure:**

**flatband voltage <> 0**
**$V_{FB}=\phi_{MS}$**




**Work functions of metal and semiconductor differ by**
$\phi_{MS} = \phi_M - \phi_S$

Energy band diagram of a metal-semiconductor system without contact (no thermal equilibrium)



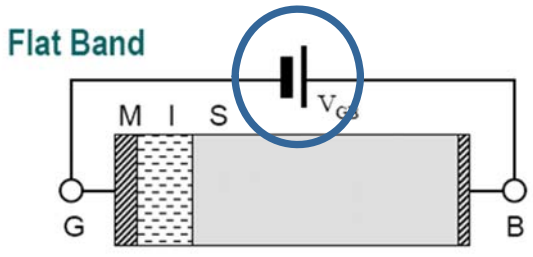

Energy band diagram of a metal-oxide-semiconductor system in contact after attaining thermal equilibrium => MOS diode



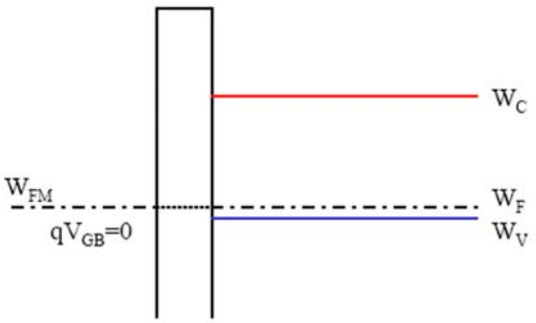


# Semiconductors physics reminder

## MOS capacitor

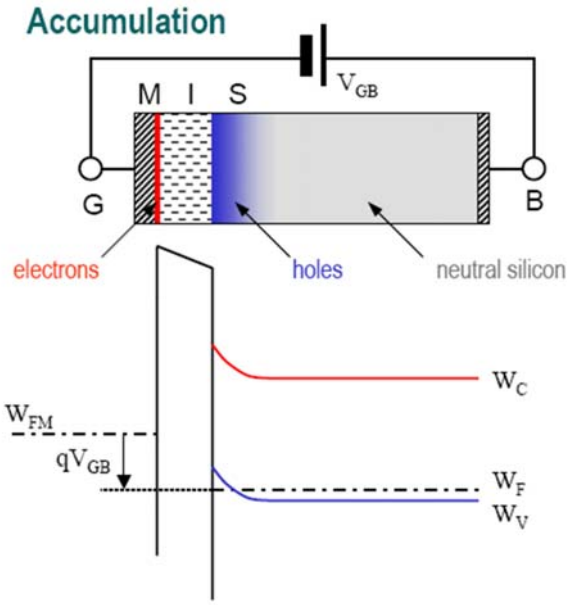



*p-type semiconductor*



# Semiconductors physics reminder

## MOS capacitor

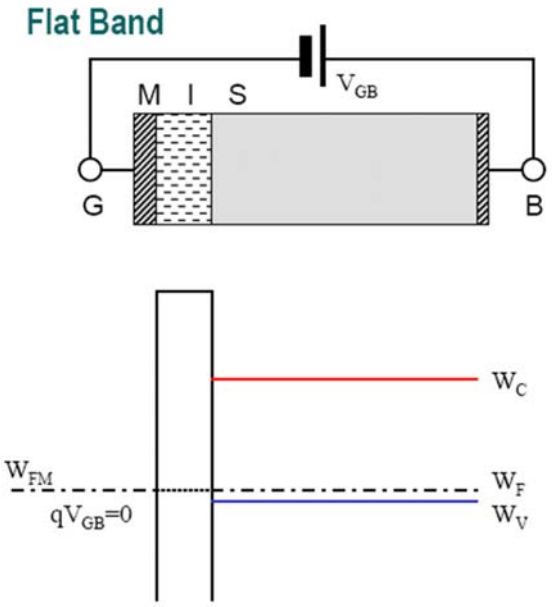





B. Föste, Infineon

# Semiconductors physics reminder

## MOS capacitor

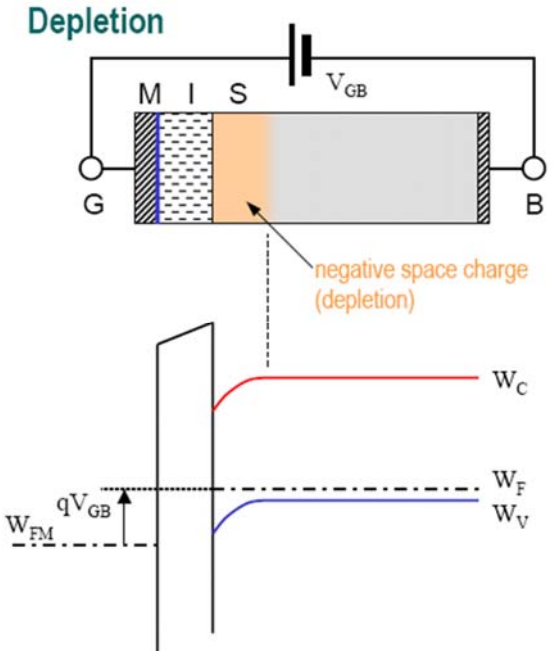





B. Föste, Infineon

# Semiconductors physics reminder

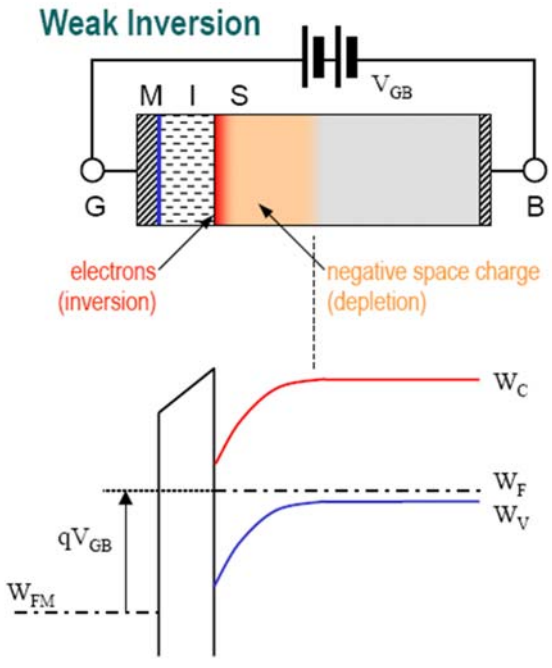
## MOS capacitor






# Semiconductors physics reminder

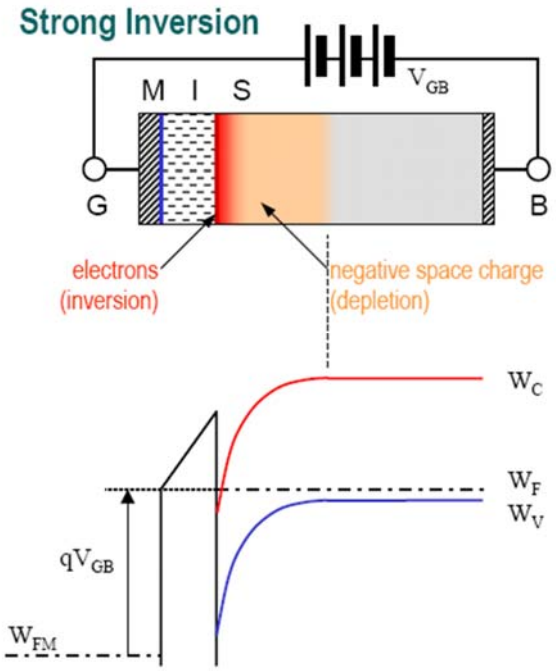
## MOS capacitor



# Semiconductors physics reminder

## MOS capacitor

**gate voltage**
⇔
control knob for charge carrier nature (electron/hole) and density at oxide/semiconductor interface

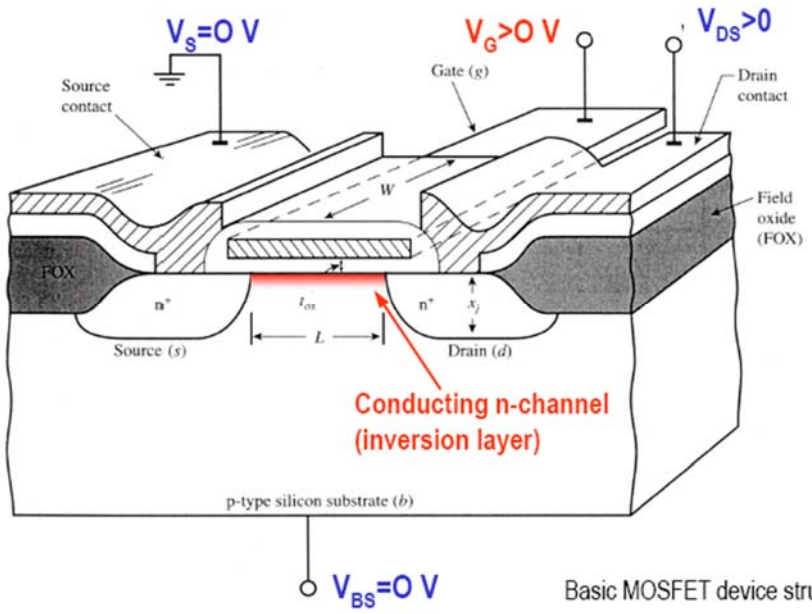





B. Föste, Infineon

# Semiconductors physics reminder

## MOSFET




Basic MOSFET device structure [*Arora*]



B. Föste, Infineon

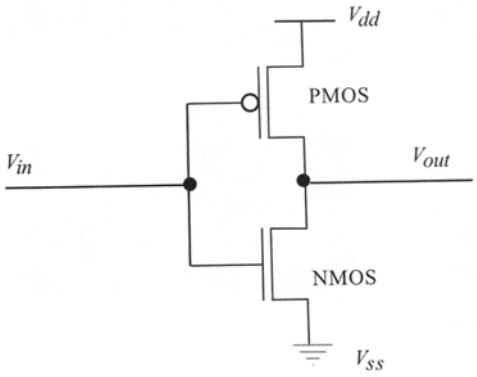
# Semiconductors physics reminder

CMOS: complementary MOS, **today's most common technology**

- n-channel MOS device in series with p-channel MOS device (when NMOS on, PMOS off and vice-versa, hence "**complementary**")
- simple design
- draws very little current (except when switched on)
- low-power technology

basic logic gate: inverter

- Vin high (1): NMOS on, PMOS off, Vout=Vss (low, 0)
- Vin low (0): NMOS off, PMOS on, Vout=Vdd (high, 1)

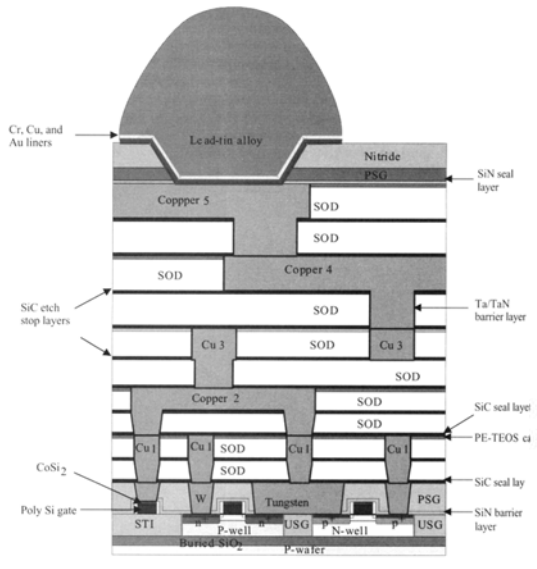


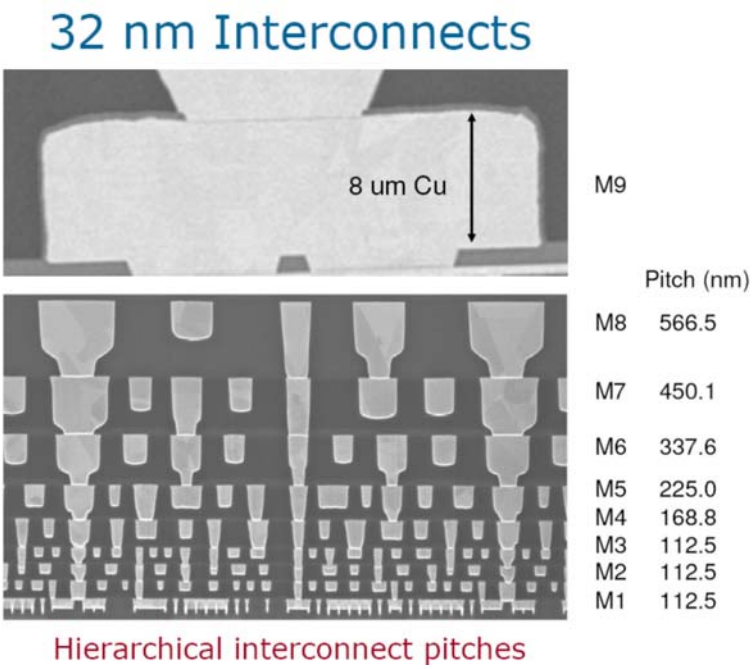



B. Föste, Infineon

# Semiconductors physics reminder

CMOS: state-of-the-art




SOI substrate, Cu/low-k interconnection,
5 metal layers, features <0.13mm, 300mm wafers (12 ")

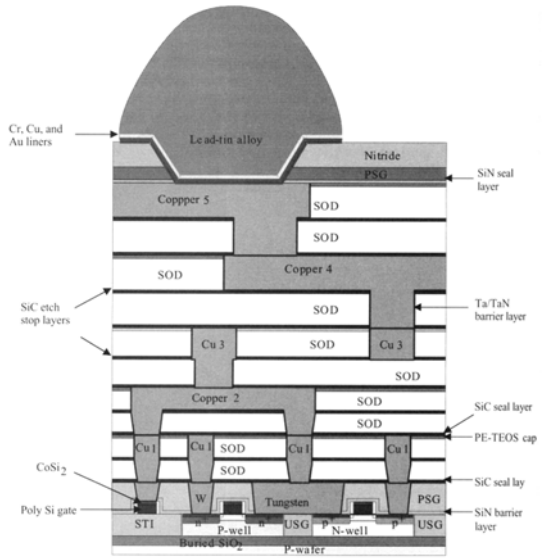


Refs 1 & 3

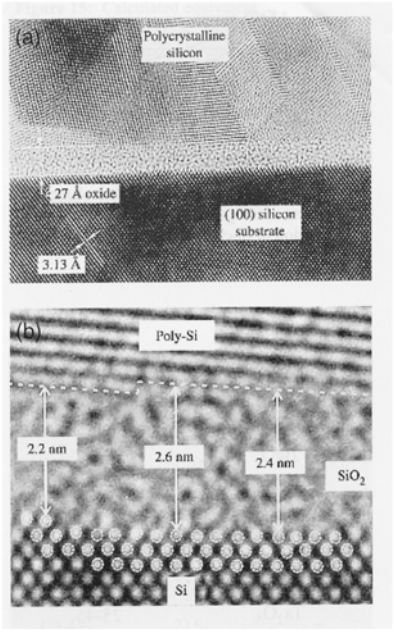
*M. Bohr, Intel*

# Semiconductors physics reminder

CMOS: state-of-the-art




SOI substrate, Cu/low-k interconnection,
5 metal layers, features <0.13mm, 300mm wafers (12 ")

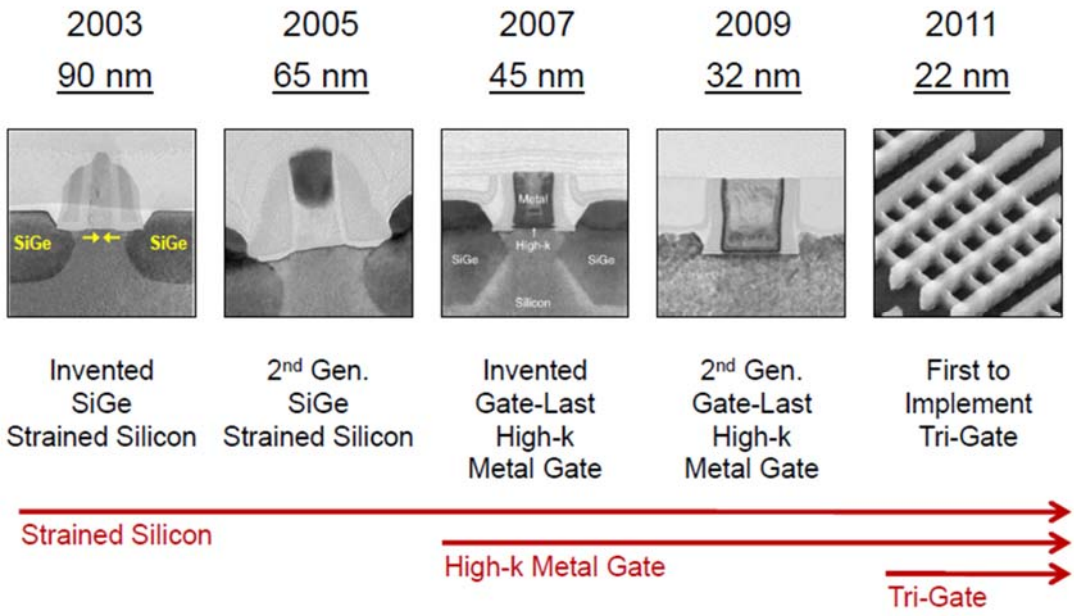



**gate structure**
very thin oxide layers



Refs 1 & 3

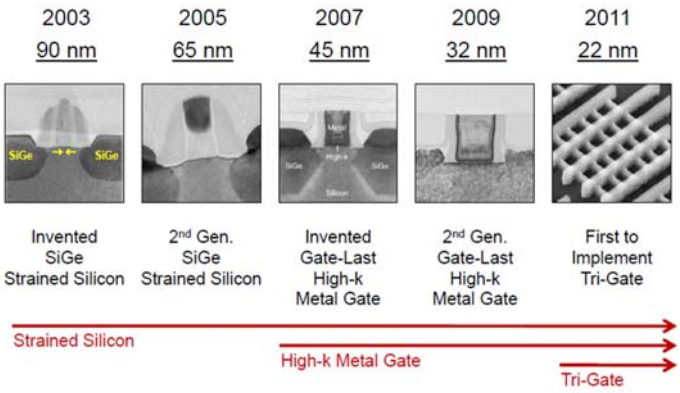
# Semiconductors physics reminder



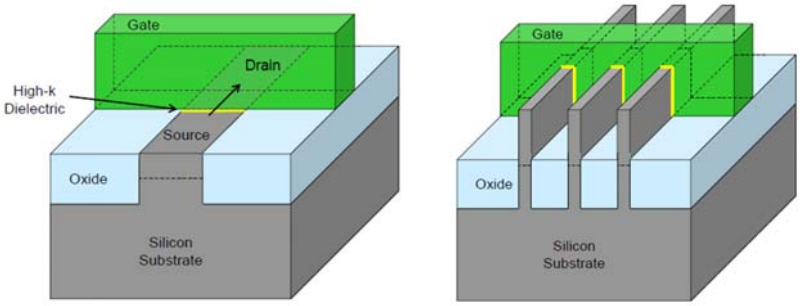



*M. Bohr, Intel*

# Semiconductors physics reminder




NB: from planar geometry to 3D geometry (fin-FETs)
also: gate all-around
*improvement of substreshold swing, higher switching speed, lower power consumption*

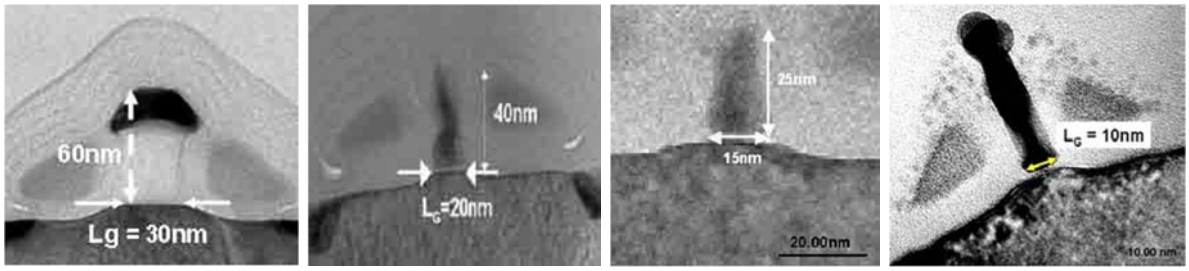




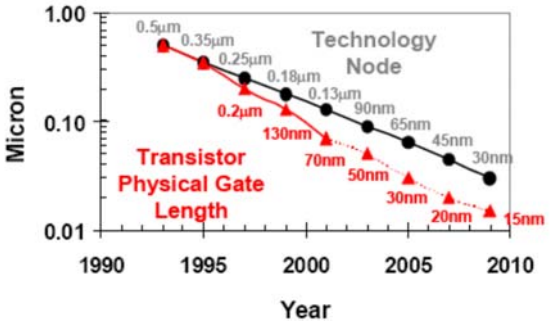

***M. Bohr, Intel***

# Semiconductors physics reminder

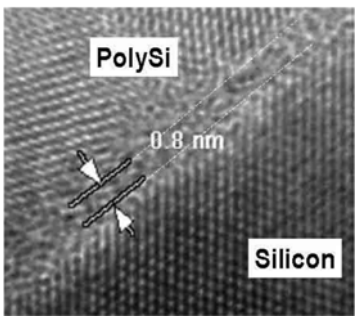
**TEM cross-sections** (Chau et al., Intel)




state-of-the-art transistors: sub-50nm technology




**gate dielectric**






***http://www.intel.com/technology/silicon/index.htm***

# Outline

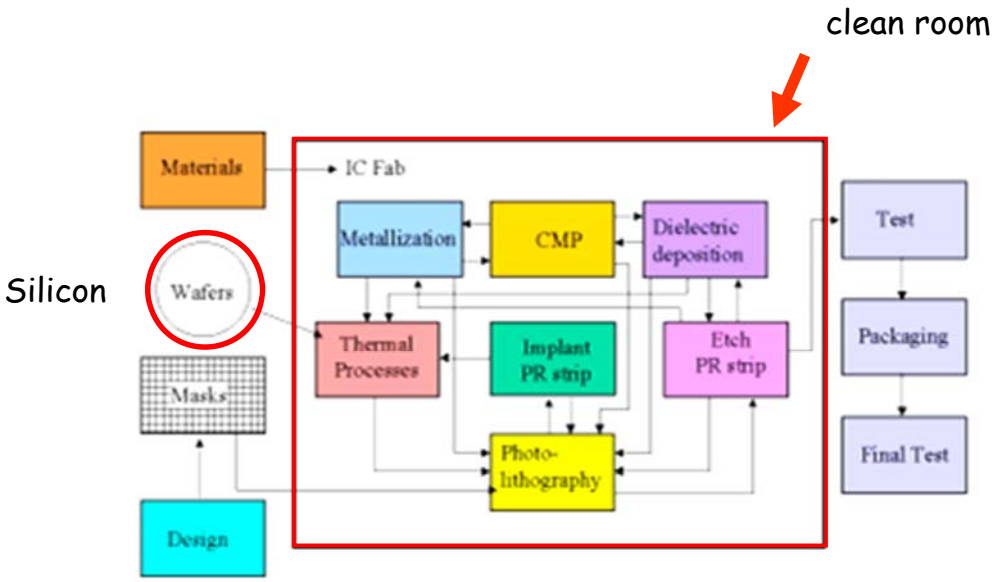
- Introduction:
  overview, state of the art,
  semiconductor physics reminder

- Fabrication basics
  - IC fabrication overview
  - clean-rooms
  - Silicon: from sand to wafer
  - material deposition techniques
  - etching
  - lithography
  - examples of devices: MEMS, NEMS

- Outlook: new and future techniques



# IC fabrication




*H. Xiao, Ref.1*

# IC fabrication

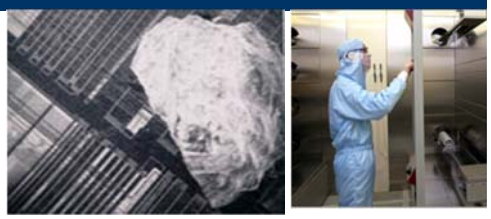
| Additive Methods | Modifying Methods | Subtractive Methods |
|---|---|---|
| **Thin Film Deposition**<br>• sputter deposition<br>• molecular beam epitaxy<br>• chemical vapor deposition<br>• chemical solution deposition | **Radiative Treatment**<br>• resist exposure<br>• polymer hardening | **Etching**<br>• wet-chemical etching<br>• ion beam etching<br>• reactive ion etching<br>• focused ion beam etching |
| **Printing Techniques**<br>• ink-jet printing<br>• microcontact printing | **Thermal Annealing**<br>• crystallization<br>• diffusion<br>• change of phase | **Radiative and Thermal Treatment**<br>• laser ablation<br>• spark erosion |
| **Self-organized Growth**<br>• selective chemical reactions<br>• biological growth of cells | **Ion Beam Treatment**<br>• implantation<br>• amorphization | **Tool-Assisted Material Removal**<br>• chemical-mechanical polishing<br>• chipping<br>• drilling<br>• milling<br>• sand blasting |
| **Assembly**<br>• wafer bonding<br>• surface mount technology<br>• wiring and bonding methods | **Mechanical Modification**<br>• plastic forming and shaping<br>• scanning probe manipulation | |



*Ref. 3*

# Clean room

grain of salt on a piece of a microprocessor

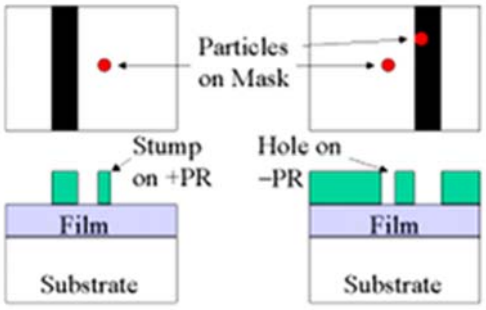


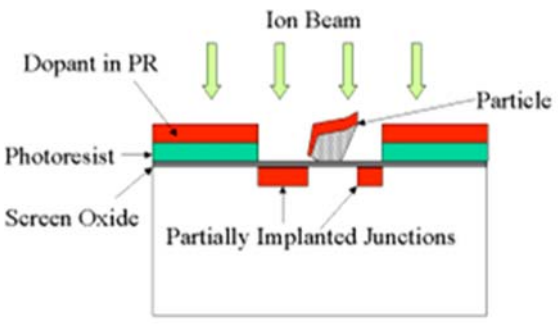
CMI, EPFL

importance of **yield** in industrial processes

➔ clean rooms

- limit contaminants
  (air, people, facility, equipment, gas, chemicals, static charges, ….)
- special furniture and tools (paper, pens, ...)



# Clean room

## clean room classes

class 1

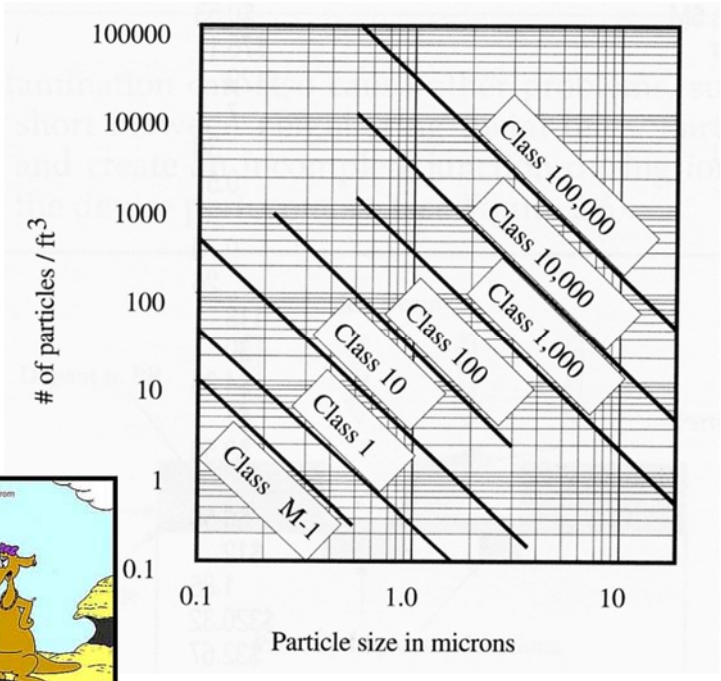
less than 1 particle of diameter larger than 0.5μm in a cubic foot

"normally clean" appartment:

typ. > 500’000 particles per cubic foot

outside air,

typ. ~ 3'000'000


*(Federal Standard 209E)*

*H. Xiao, Ref.1*



# Clean room

| Class | maximum particles/ft³ | | | | | ISO equivalent |
|---|---|---|---|---|---|---|
| | ≥0.1 μm | ≥0.2 μm | ≥0.3 μm | ≥0.5 μm | ≥5 μm | |
| **1** | 35 | 7 | 3 | 1 | | ISO 3 |
| **10** | 350 | 75 | 30 | 10 | | ISO 4 |
| **100** | | 750 | 300 | 100 | | ISO 5 |
| **1,000** | | | | 1,000 | 7 | ISO 6 |
| **10,000** | | | | 10,000 | 70 | ISO 7 |
| **100,000** | | | | 100,000 | 700 | ISO 8 |

**clean room standard** (ISO 14644-1)

$Cn = 10^N (0.1 / D)^{2.08}$

| | |
|---|---|
| Cn | maximum permitted number of particles per $m^3$ ≥ specified particle size (rounded) |
| N | ISO class number ( multiple of 0.1 and ≤ 9) |
| D | particle size (micrometers) |

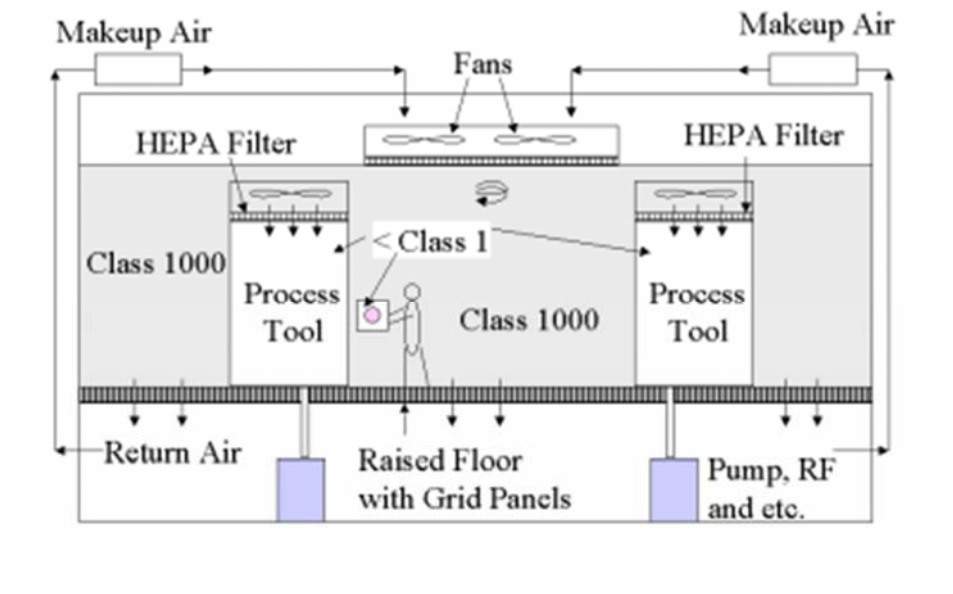
# Clean room

| Particle | Particle Size *(microns)* |
|---|---|
| Beach Sand | 100 - 10000 |
| Pollens | 10 - 1000 |
| Textile Fibers | 10 - 1000 |
| Human Hair | 40 - 300 |
| Saw Dust | 30 - 600 |
| Tea Dust | 8 - 300 |
| Red Blood Cells | 5 - 10 |
| Spores | 3 - 40 |
| Coal Dust | 1 - 100 |
| Smoke from Synthetic Materials | 1 - 50 |
| Auto and Car Emission | 1 - 150 |
| Metallurgical Dust | 0.1 - 1000 |
| Humidifier | 0.9 - 3 |
| Copier Toner | 0.5 - 15 |
| Bacteria | 0.3 - 60 |
| Burning Wood | 0.2 - 3 |
| Tobacco Smoke | 0.01 - 4 |
| Viruses | 0.005 - 0.3 |
| Typical Atmospheric Dust | 0.001 to 30 |



# Clean room

## simple clean room design

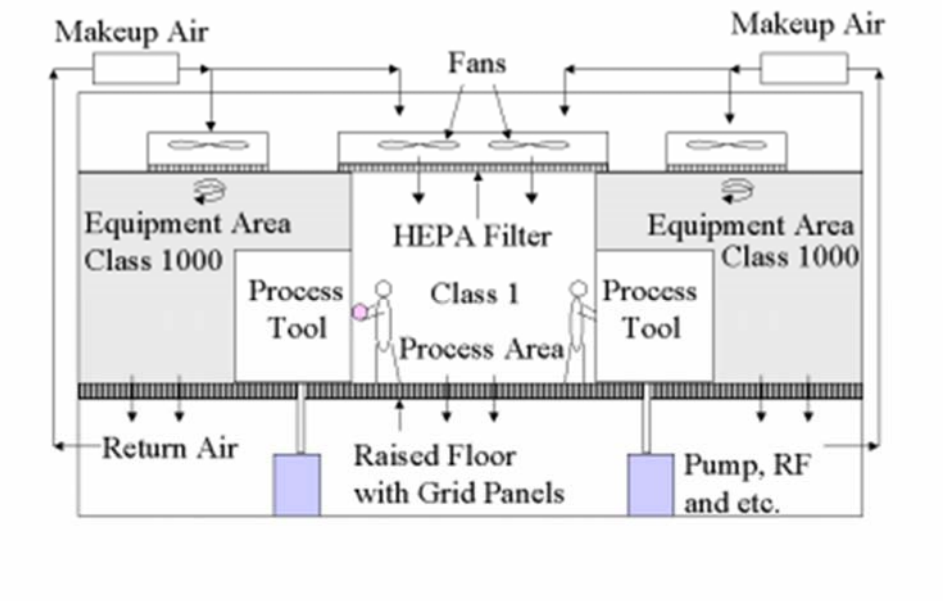





*H. Xiao, Ref.1*

# Clean room

## more advanced clean room design




*H. Xiao, Ref.1*



# Clean room


## Steps to enter a cleanroom (Intel)

1. Store personal items.
2. Discard any gum, candy, etc.
3. Remove any makeup with cleanroom soap and water.
4. ***Take a drink of water to wash away throat particles.***
5. Cover any facial hair with a surgical mask or beard/mustache lint-free cover.
6. Put on a lint-free head cover.
7. Clean shoes with shoe cleaners.
8. Put shoe cover on over shoes.
9. Clean any small, pre-approved items to be taken inside.
10. Pick up booties.
11. Sit on "dirty" side of bench.
12. Put on one bootie (over plastic shoe cover).
13. Swing bootied foot to "clean" side of bench.
14. Put on other bootie on "dirty" side.
15. Swing bootied foot to "clean" side.
16. Enter main gowning room.
17. Set aside badge, pager, and any other items to be taken inside.
18. Put on nylon gowning gloves.
19. Obtain bunny suit and belt from hanger.
21. If you've never done it before, putting on a bunny suit can take 30 to 40 minutes. The Intel pros can do it in five.
22. Put on bunny suit without letting it touch the floor.
23. Put on belt.
24. Tuck bunny suit pant legs into booties.
25. Fasten snaps at top of booties.
26. Attach filter unit to belt.
27. Attach battery pack to belt.
28. Plug filter unit into battery pack.
29. Obtain helmet, safety glasses, and ID badge from rack.
30. Put on helmet.
31. Tuck helmet skirt into bunny suit.

http://www.intel.com/

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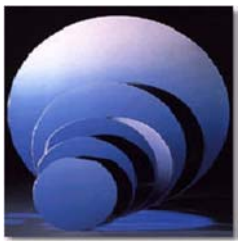
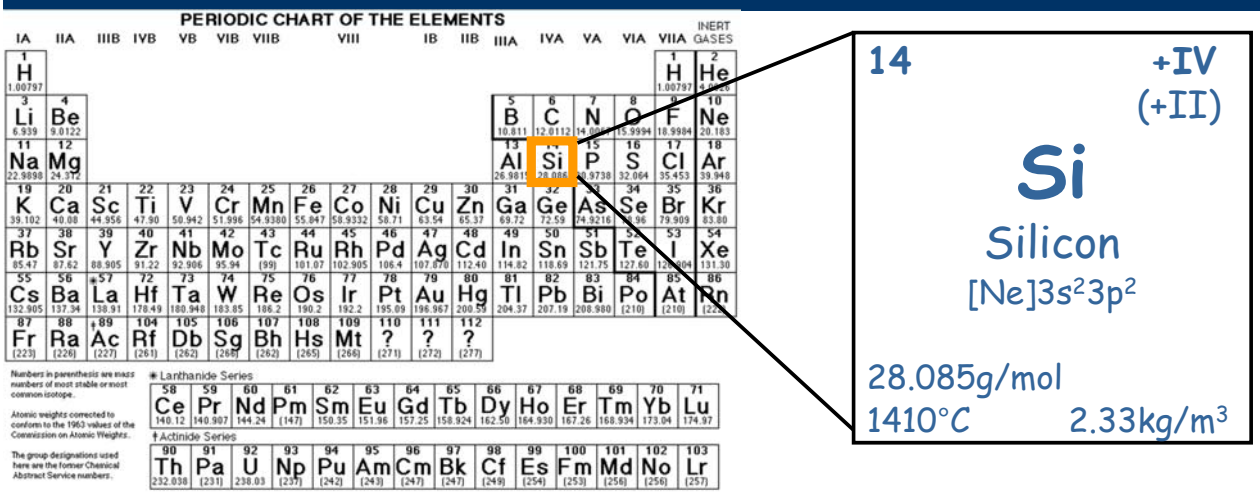




# Silicon: from sand to wafer




2nd (after oxygen) most abundant in earth's crusts: 26%

7th most abundant element in universe

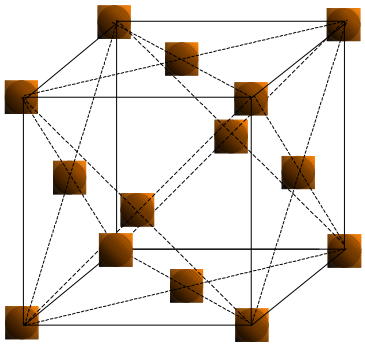
# Silicon: from sand to wafer

Si: nonmetallic element, indirect semiconductor

| | |
|---|---|
| $SiO_2$ | glass (amorphous), quartz (cristalline) |
| SiC | very hard (polishing) |
| Si | crystalline (semiconductor industry) |

typical resistivity: 100 mΩ cm

structure: cfc (diamond-like)




Amorphous | Polycrystalline | Single crystal



*C. Heedt, Wacker Siltronic*

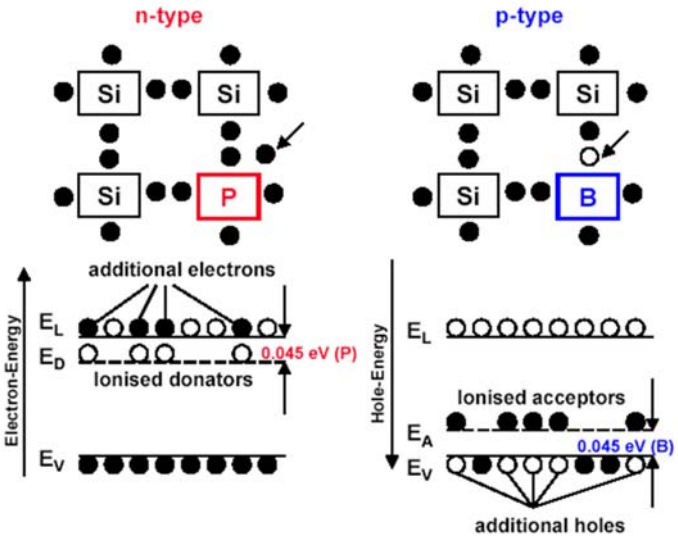
# Silicon: from sand to wafer

advantadges of Si over other semiconductors (Ge)

- cheap, abundant
- **oxide ($SiO_2$) strong and stable dielectric** (⇨ MOS technology); grown easily by thermal oxidation
- larger band gap (1.1 eV): higher operation T
- larger breakdown voltage

Doping elements

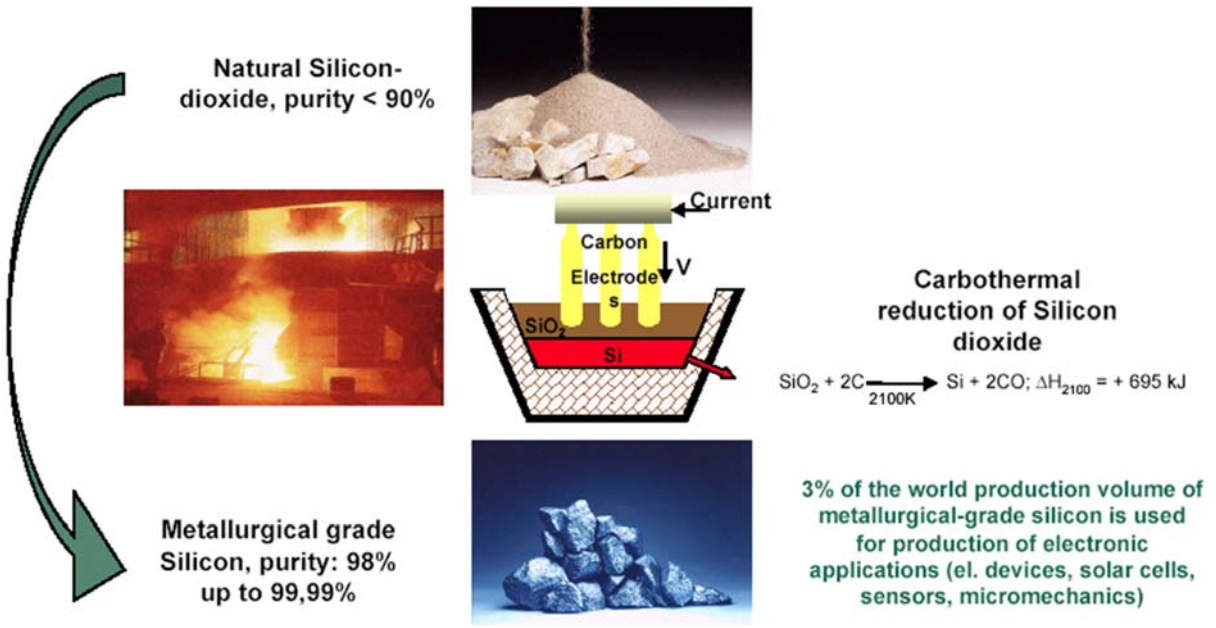
- n-type: P (phophorus), As (arsenic), Sb (antimony)
- p-type: B (boron)



# Silicon: from sand to wafer

Si purification: natural Si oxide ➔ MGS ➔ EGS

metallurgical electronic grade

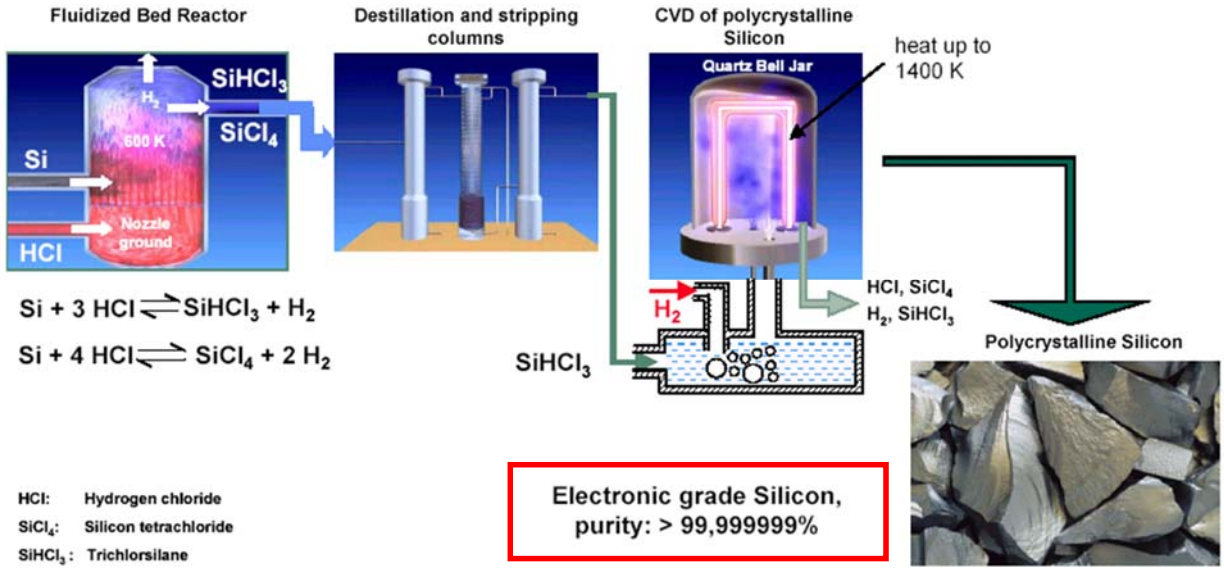





*C. Heedt, Wacker Siltronic*

# Silicon: from sand to wafer

Si purification: MGS ➔ EGS

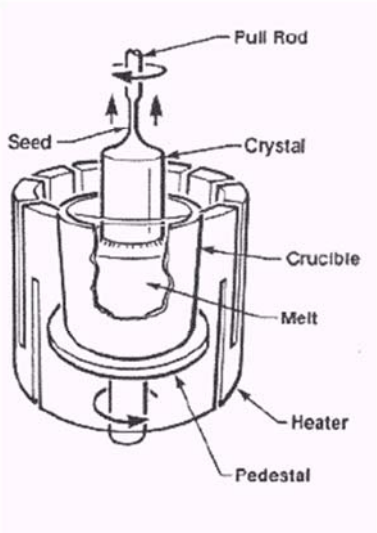





*C. Heedt, Wacker Siltronic*

# Silicon: from sand to wafer

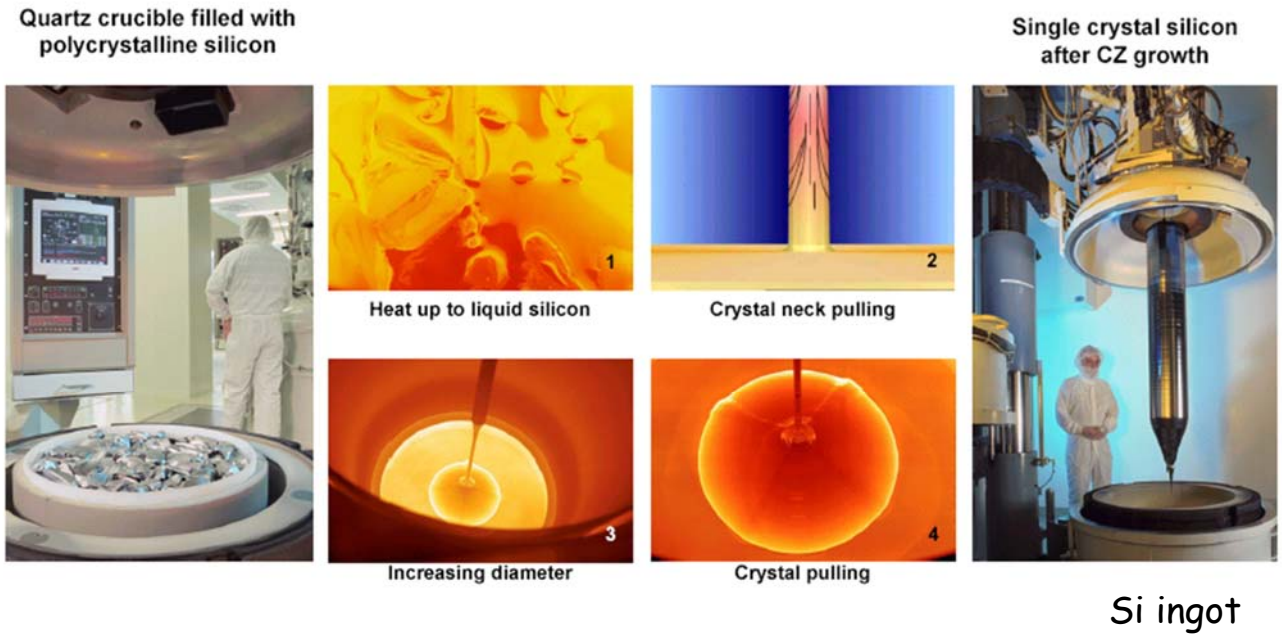
EGS ➔ single cristal ingot: CZ growth (Czochralski method)






*C. Heedt, Wacker Siltronic*

# Silicon: from sand to wafer




Si ingot

up to 300mm diameter (FZ or floating zone purer butlimited to 200mm)



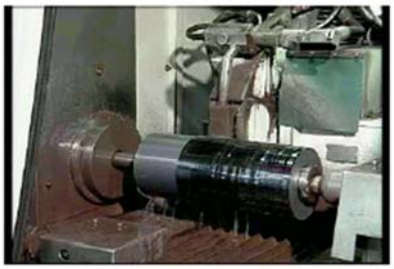
*C. Heedt, Wacker Siltronic*

# Silicon: from sand to wafer

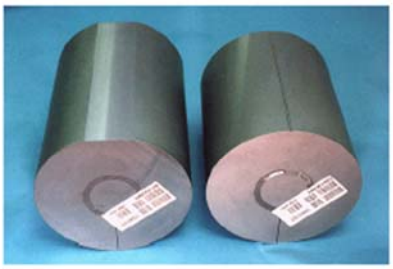
## Surface grinding

mark crist. orient.

Cut the ingot in defined length



Ground to cylindrical diameter



Ground flat or notch

flat: up to 150mm

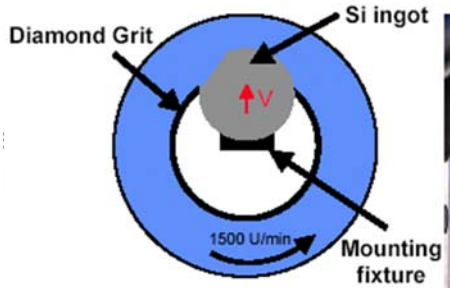
notch: > 200mm

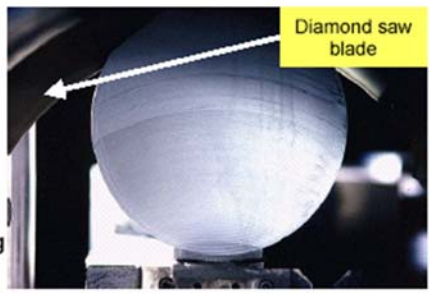


*C. Heedt, Wacker Siltronic*

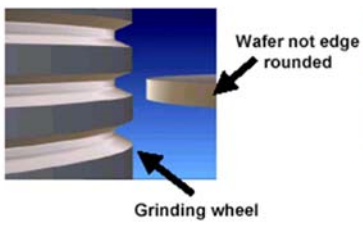
# Silicon: from sand to wafer

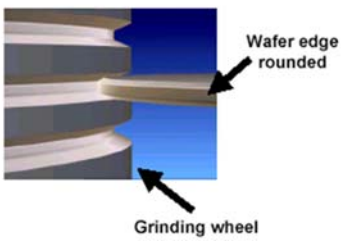
## wafer sawing

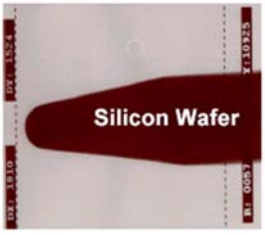



## edge rounding





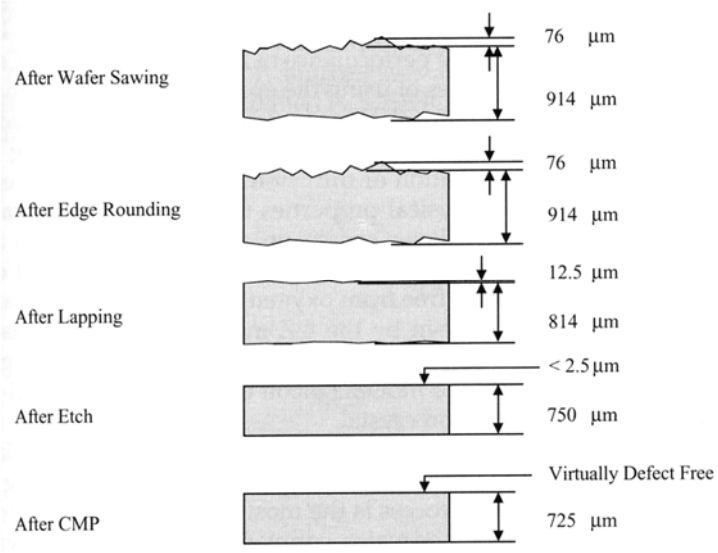

*C. Heedt, Wacker Siltronic*

# Silicon: from sand to wafer

## wafer finishing

- lapping
  (global planarization, double-sided)
- wet etching , isotropic
  (4:1:3 mixture of $HNO_3$, HF and $CH_3COOH$)
- CMP (chemical mechanical polishing)
- wet cleaning (RCA1, RCA2)

surface roughness after the various treatment





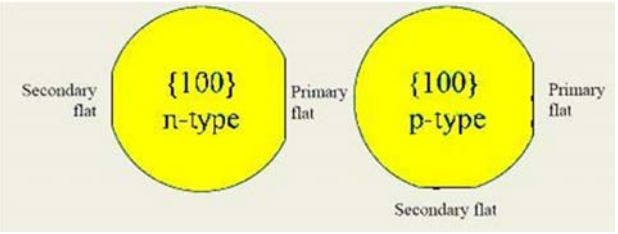

# Silicon: from sand to wafer

## wafer flats

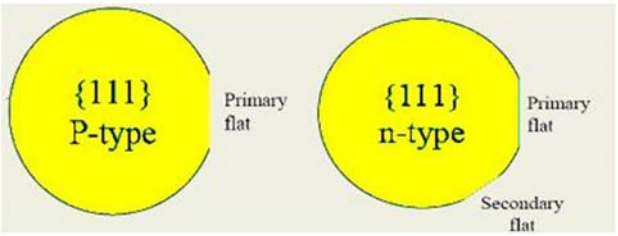
- Orientation for automatic equipment
- Indicate type and orientation of crystal.

**Primary flat** – The flat of longest length located in the circumference of the wafer. The primary flat has a specific crystal orientation relative to the wafer surface.

**Secondary flat** – Indicates the crystal orientation and doping of the wafer. The location of this flat varies.




**flat at 180 deg for n-type and 90 deg for p-type**



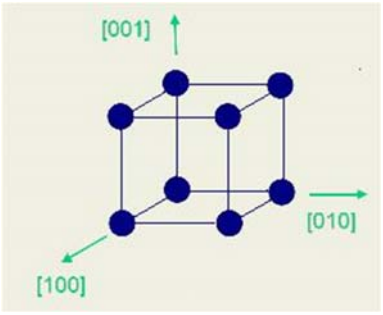

**flat at 45 deg for n-type, no secondary for p-type**

# Silicon: from sand to wafer

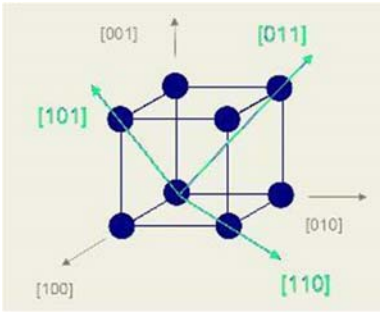
**Miller indices** description of lattice planes and lattice directions in crystal

example **cubic lattice system**

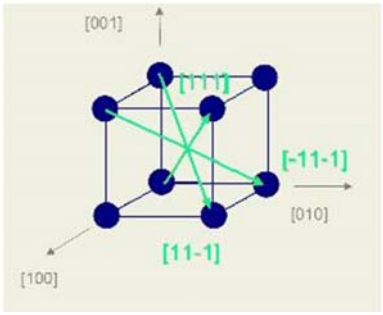
the direction [hkl] defines a vector direction normal to surface of a particular plane or facet.




**type: <100>**
**Equivalent directions:**
**[100],[010],[001]**




**type: <110>**
**Equivalent directions:**
**[110], [011], [101],**
**[-1-10], [0-1-1], [-10-1],**
**[-110], [0-11], [-101],**
**[1-10], [01-1], [10-1]**




**type: <111>**
**Equivalent directions:**
**[111], [-111], [1-11], [11-1]**



# Outline

- Introduction:
  overview, state of the art,
  semiconductor physics reminder

- Fabrication basics
  - IC fabrication overview
  - clean-rooms
  - Silicon: from sand to wafer

**additive** → material deposition techniques

substractive → etching

  - lithography
  - examples of devices: MEMS, NEMS

- Outlook: new and future techniques

# Fabrication: physical deposition techniques

**fundamentals of film deposition**

- gas kinetics
  (mean free path: small holes filling, residual gas atoms: purity)
- UHV ($p<10^{-9}$ mbar) necessary depending on final purity needed
- phase diagrams of materials to deposit (pressure, temperature)
- control type of growth: homoepitaxy; heteroepitaxy; growth of polycristalline or amorphous layers;
  importance of strain ➔ misfit dislocations
  substrate temperature



# Fabrication: physical deposition techniques

- gas kinetics
  (mean free path: small holes filling, residual gas atoms: purity)

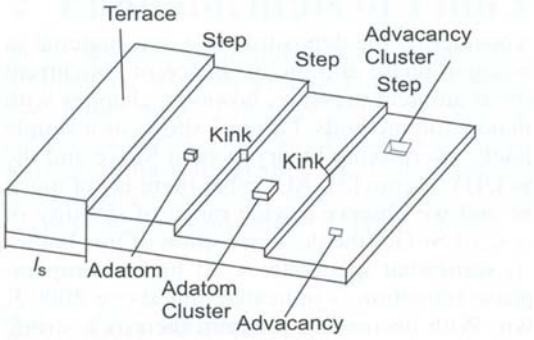
table for residual air at 25°C

| $p$, mbar | Mean free path, cm (between collisions) | Collisions / s (between molecules) | Molecules/(cm² s) (sticking surface) | Monolayer / s |
|---|---|---|---|---|
| $10^{0}$ | $6.8\cdot10^{-3}$ | $6.7\cdot10^{6}$ | $2.8\cdot10^{20}$ | $3.3\cdot10^{5}$ |
| $10^{-3}$ | $6.8\cdot10^{0}$ | $6.7\cdot10^{3}$ | $2.8\cdot10^{17}$ | $3.3\cdot10^{2}$ |
| $10^{-6}$ | $6.8\cdot10^{3}$ | $6.7\cdot10^{0}$ | $2.8\cdot10^{14}$ | $3.3\cdot10^{-1}$ |
| $10^{-9}$ | $6.8\cdot10^{6}$ | $6.7\cdot10^{-3}$ | $2.8\cdot10^{11}$ | $3.3\cdot10^{-4}$ |

surface= 1cm$^2$

# Fabrication: physical deposition techniques

- type of growth: homoepitaxy




***IBM Almaden***
*STM image, 28nm by 28nm area of the terraced copper and copper nitride surface with Manganese humps (1-10 atoms long).*

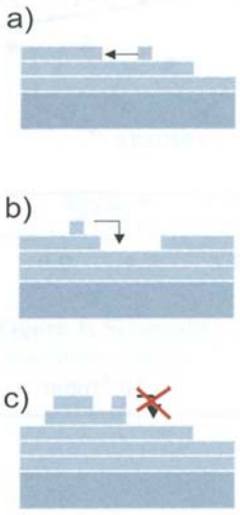
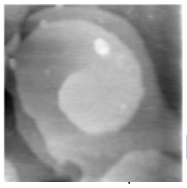



**Figure 7:** Growth modes of homoepitaxy: (a) step-propagation, (b) 2d-island growth, and (c) multi-layer growth.



# Fabrication: physical deposition techniques

- heteroepitaxy

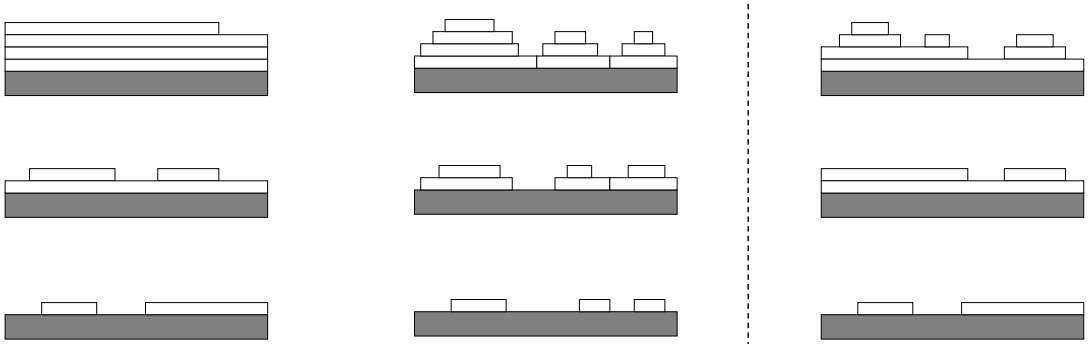


small mismatch — large mismatch

Frank-Van der Merwe
(layer growth; ideal)

Volmer-Weber
(island growth)

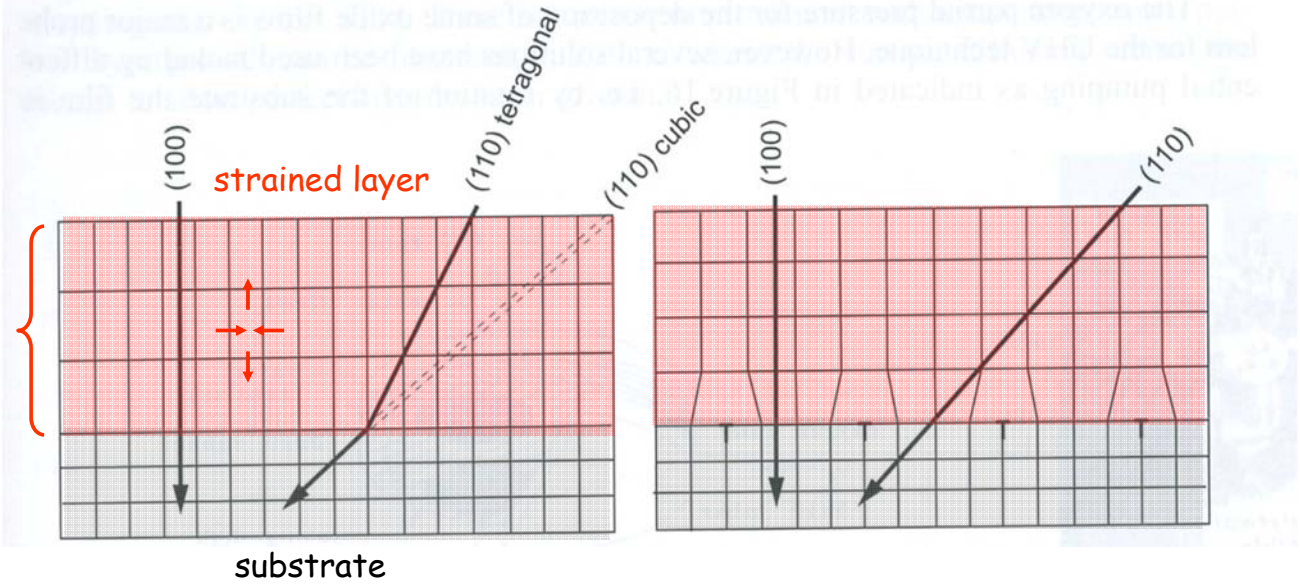
Stranski-Krastanov
(layers then islands due to strain build up)



# Fabrication: physical deposition techniques

- importance of strain

➔ misfit dislocations: **T**






# Fabrication: physical deposition techniques

example of the importance of strain

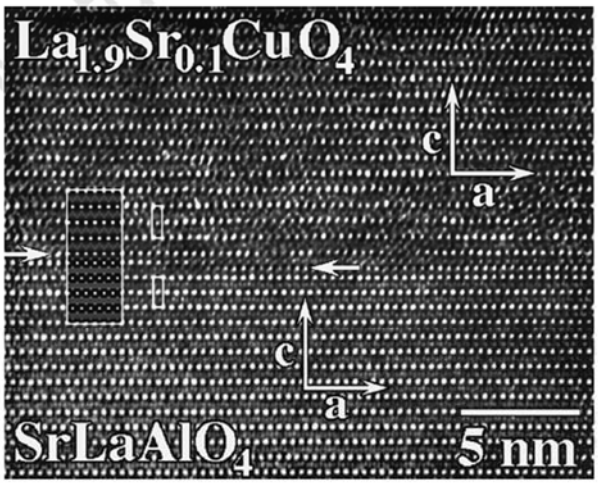
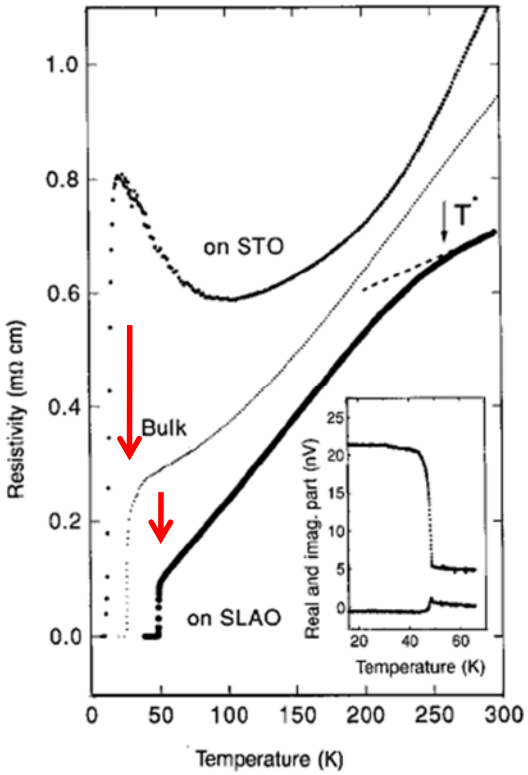


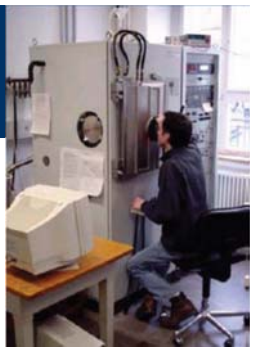

**Figure 3** Cross-section, high-resolution electron-microscopy image of the '214' film on SLAO. On the basis of image simulations, the white dots in the film and substrate can be correlated with Cu and Al columns, respectively. The unit cells are indicated by the small white rectangles. The inset shows the simulated image of the interface structure with the stacking sequence LaO-LaO-$AlO_2$-LaO-$CuO_2$-LaO-LaO.






*Locquet, Perret et al., Nature 1998*

# Fabrication: thermal evaporation

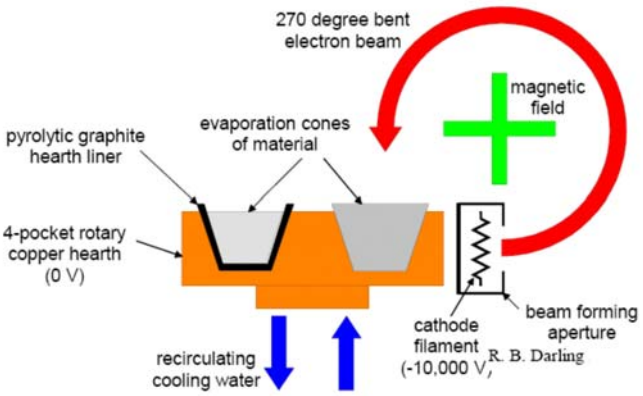


## thermal evaporation: free, isotropic (Langmuir)

### e-beam evaporation

- More complex, but extremely versatile.
- **T > ~ 3000°C**
- Use evaporation cones or crucibles (e.g. graphite) in a copper hearth.
- Typical emission voltage is 8-10 kV.
- Exposes substrates to secondary electron radiation.
  *(X-rays can also be generated by high voltage electron beam)*

- **Typical deposition rates are 1-100 Å/s**
- Common evaporant materials:
  – Everything a resistance heated evaporator will accommodate, plus:
  – Ni, Pt, Ir, Rh, Ti, V, Zr, W, Ta, Mo
  – Al2O3, SiO, SiO2, SnO2, TiO2, ZrO2






# Fabrication: thermal evaporation

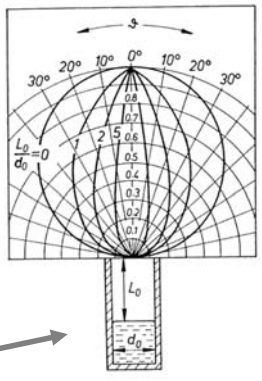
## thermal evaporation: ~ directional

### effusion (Knudsen) cell

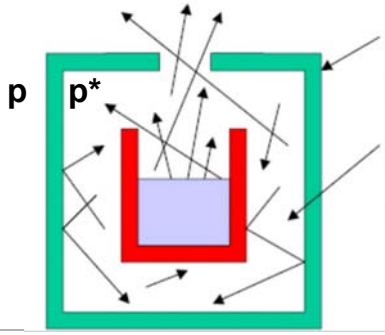
evaporation rate ~ controlled by **temperature** only
*(play with equilibrium vapor pressure and aperture size)*

**Kn=λ/d** λ: mean free path, d: orifice diameter

Kn>1 free molecular flow
kn<<1 viscous flow




NB: distribution of vapor beam intensity; depends on **ratio L/d** (filling level of cell !)




Isothermal enclosure with a small orifice of area $A_e$.

Surface area of the evaporant inside the enclosure is large compared to the area of the orifice.

An equilibrium vapor pressure P* is maintained inside the enclosure.

Effusion from a Knudsen cell is therefore:

$$\frac{dN_e}{dt} = A_e\left(2\pi m k_B T\right)^{-1/2}\left(P^* - P\right)$$

*Biasiol and Sorbia, 2001*

# Fabrication: physical deposition techniques

## NB: shadow effects / step coverage

⇨ directionality and adhesion effects

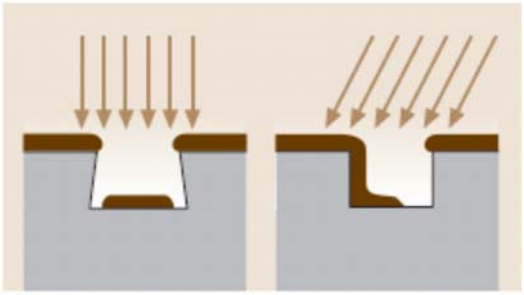


Fig. 5.8 Shadow effects observed in evaporated films. *Arrows* show the trajectory of the material atoms being deposited

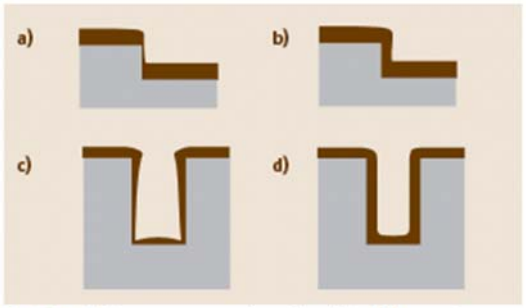
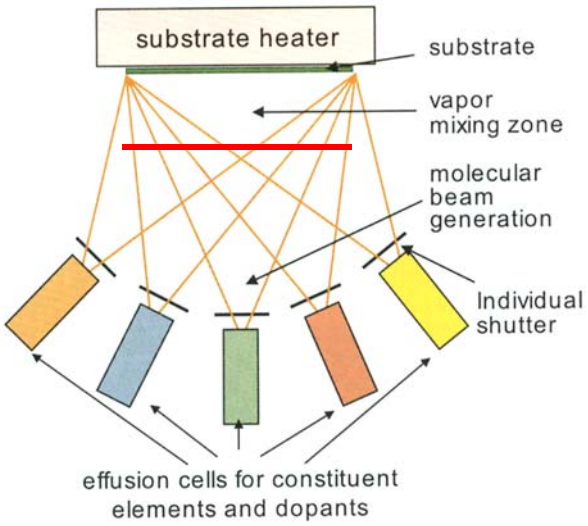



Fig. 5.3a–d Step coverage and conformality: (a) poor step coverage, (b) good step coverage, (c) nonconformal layer, and (d) conformal layer

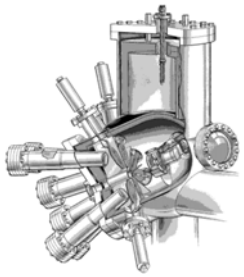


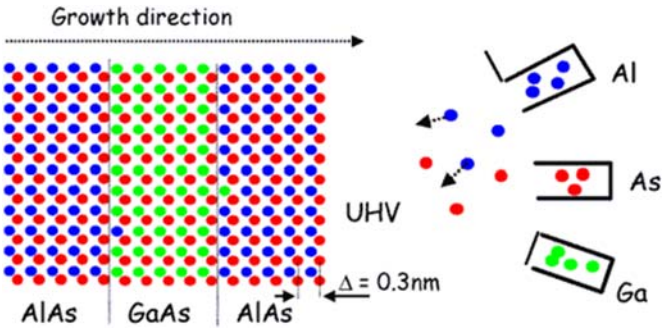
*Springer Handbook of nanotechnology, Bushan ed., 2004*

# Fabrication: Molecular Beam Epitaxy (MBE)




- source: effusion cells
- multiple cells/shutters
- UHV (⇨ *in-situ* surface characterisation techniques possible)
- epitaxy (heated substrate)





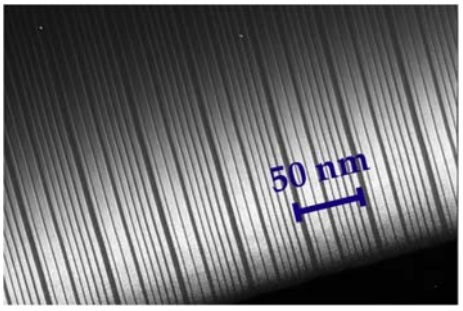

excellent control on layer compostion

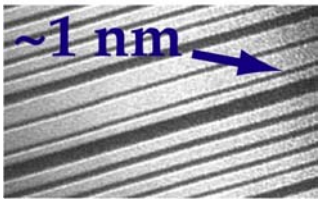


*Ref. 3 & J.Faist*

# Fabrication: Molecular Beam Epitaxy (MBE)

## Molecular Beam Epitaxy (MBE)



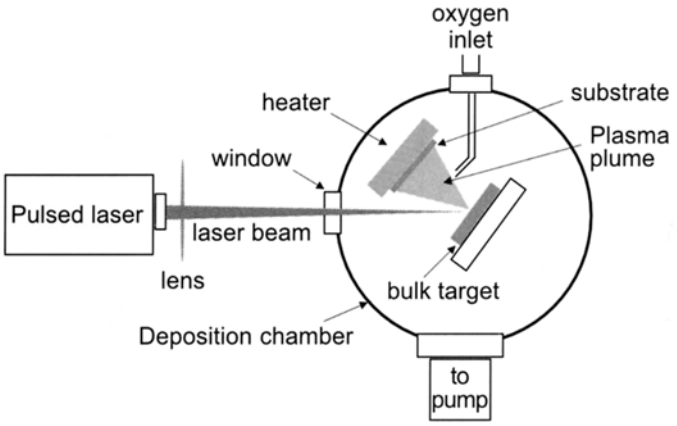




TEM pictures of a QCL GaAs/AlGaAs structure (J. Faist, ETHZ)

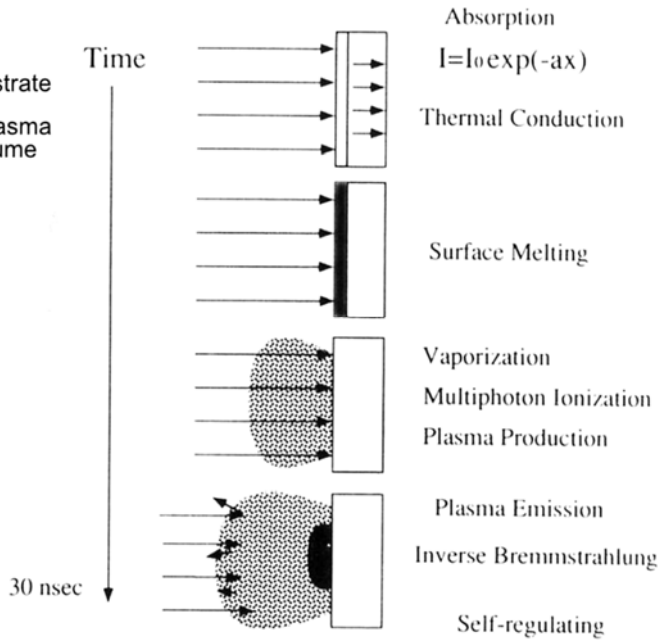


*J.Faist, ETHZ*

# Fabrication: Pulsed Laser Deposition (PLD), laser ablation




- source: target, thermal energy (laser pulse ~ few J/cm$^2$)
- multiple target possible (YBCO/PBCO)
- typ. oxide films
- epitaxy (heated substrate)
- off-axis geometry (rotating substrate)
- stoechiometric transfer



# Fabrication: Sputtering

## DC sputtering

- few 100V ➔ plasma (p~$10^{-1}$ - $10^{-3}$mbar)
- sputtering of target by ions, typ. $Ar^+$
  (binding energy of target atoms: 4-8eV; min energy of $Ar^+$ ions: 20-50eV; multiple collisions necessary to get backward material)
- stoichiometry of target (~) preserved
- increase ionization rate of plasma with B-field (magnetron sputtering)
- insulating targets: RF-sputtering (~13MHz)

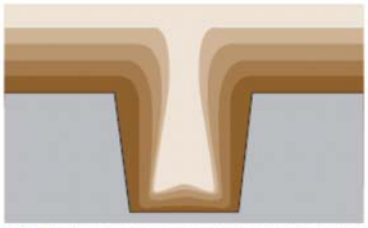
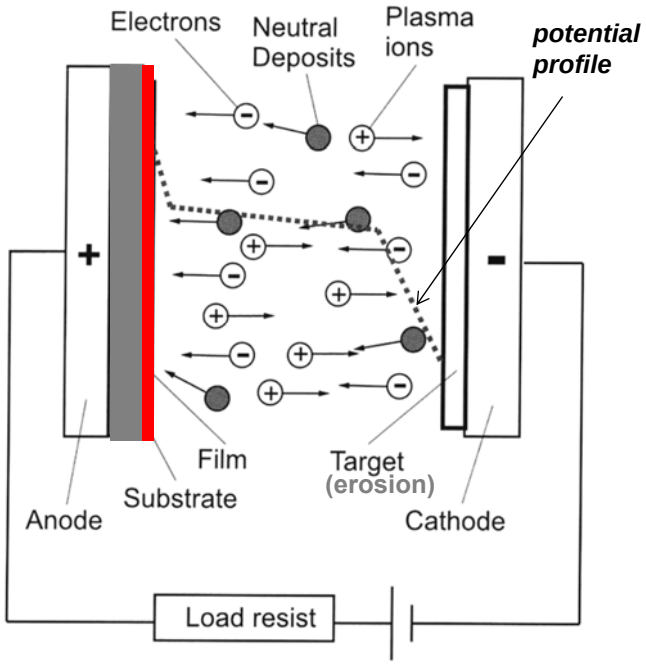


Fig. 5.9 Typical cross section evolution of a trench while being filled with sputter deposition






# Fabrication: Chemical Vapor Deposition

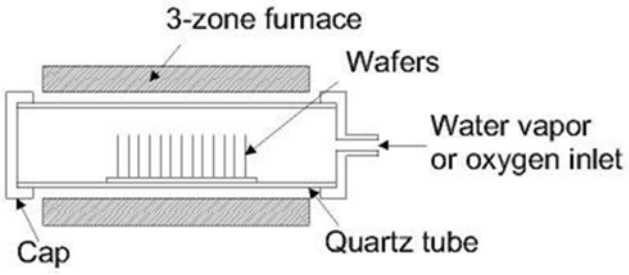
## Chemical Vapor Deposition **(CVD)**

CMI, EPFL

**def**: reaction of chemicals (precursors, gas phase) at high T to form the deposited thin film

| | | | |
|---|---|---|---|
| **SiO2** | $3\ SiH_4 + O_2$ | ⇨ $SiO_2 + 2\ H_2$ | 450°C |
| **SiO2** | $SiCl_2H_2 + 2N_2O$ | ⇨ $SiO_2 + 2\ N_2 + 2HCl$ | 900°C |
| **Si3N4** | $3\ SiH_4 + 4NH_3$ | ⇨ $Si_3N_4 + 12\ H_2$ | 700°C-900°C |
| **poly Si** | $SiH_4$ | ⇨ $Si + 2\ H_2$ | 580-650°C, 1mbar |

note: **stress** can be critical (e.g. nitride layers)




**LPCVD**: low-pressure CVD; requires higher temperatures
**PECVD**: plasma enhanced CVD, allows temperature reduction
**MOCVD**: metal-organic CVD, use organometallic precursors

# Fabrication: chemical deposition techniques

note: **thermal oxidation**

(note really a deposition process, Si consumed during process)

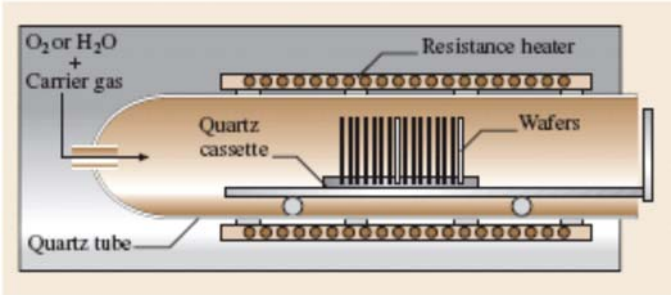
⇨ better oxide quality, very low density of defects, homogeneous thickness (**gate –** insulating **-** material)

**dry** Si (solid) + $O_2$ (gas) ⇨ $SiO_2$ (solid)

**wet** Si (solid) + $H_2O$ (steam) ⇨ $SiO_2$ (solid) + $2H_2$ (gas)

final thickness: few x 10Å to 2μm (NB: native oxide layer: ~ 2nm)

**T ~ 900°C – 1200°C**




limited to materials able to form oxides

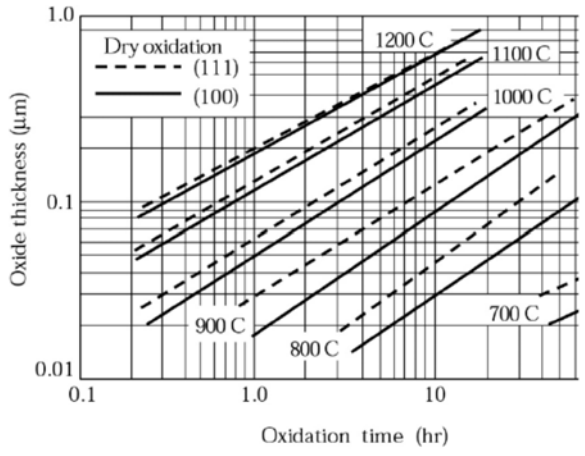


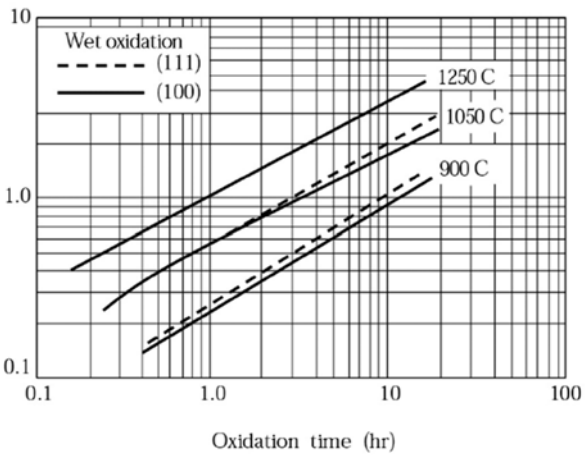
# Fabrication: chemical deposition techniques

**thermal oxidation**

$$x_{ox}(t) \propto [1+c(t+\tau)]^{1/2}$$

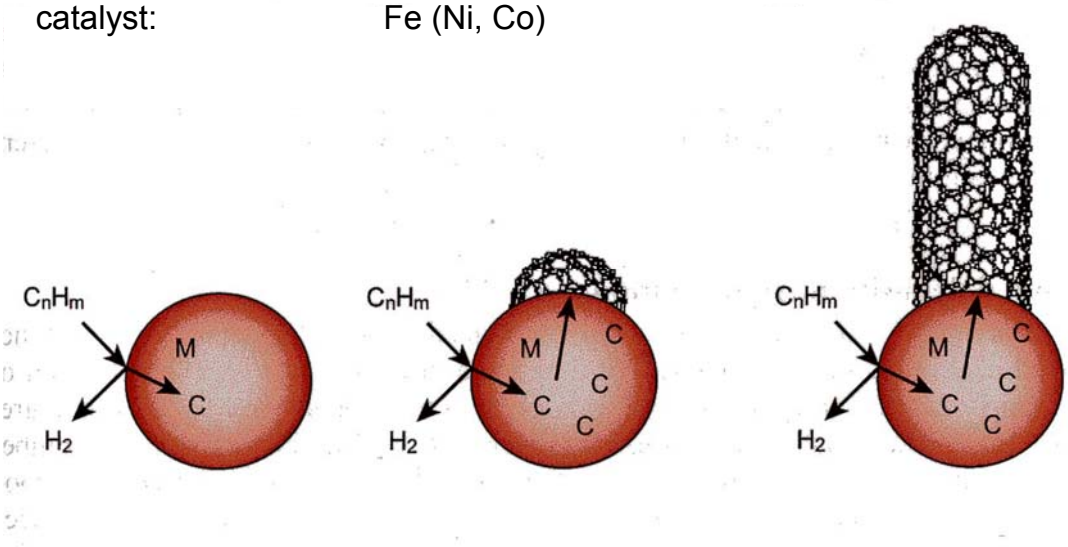
***(Deal-Grove)***



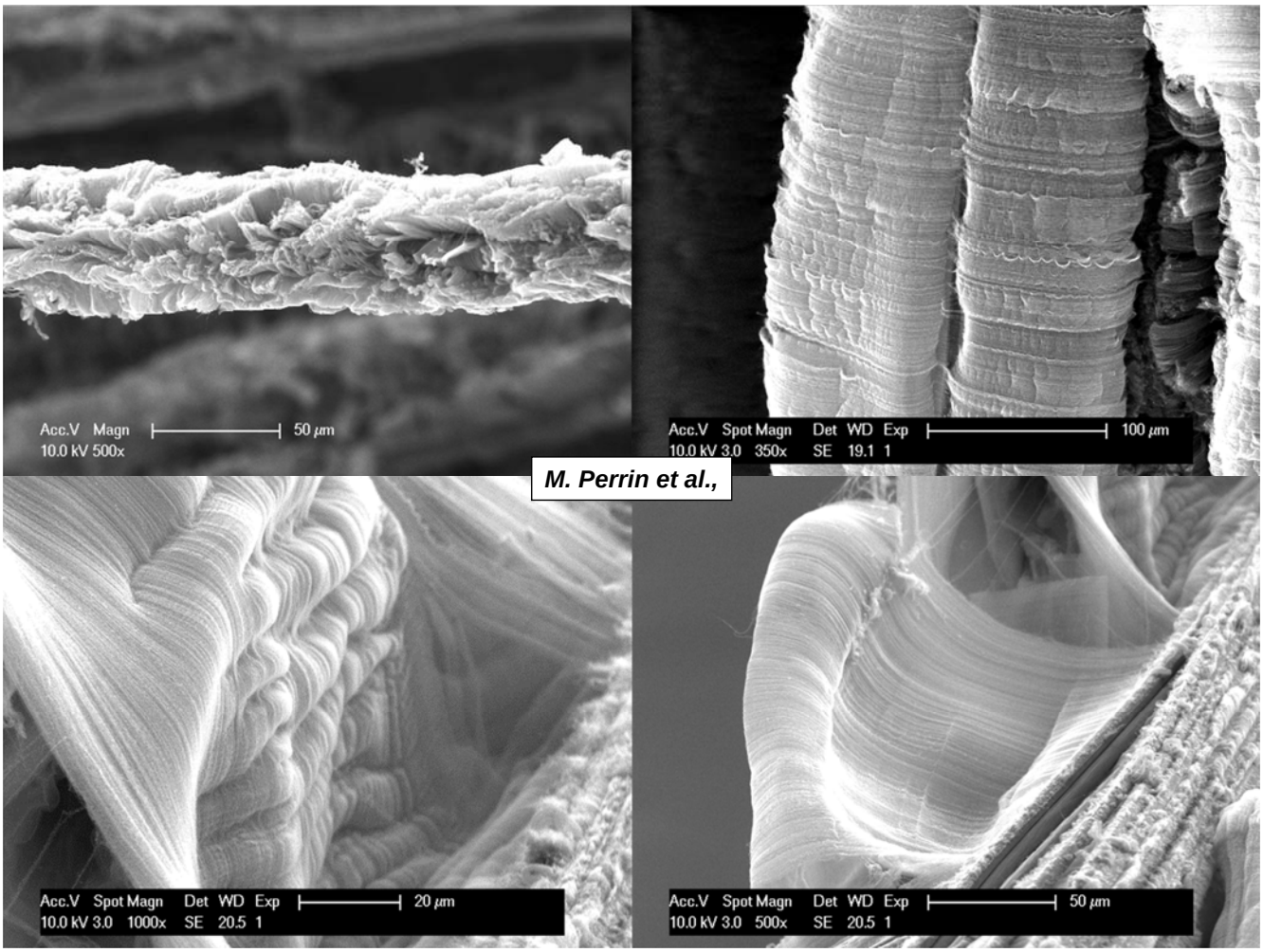



# CVD example: CNTs

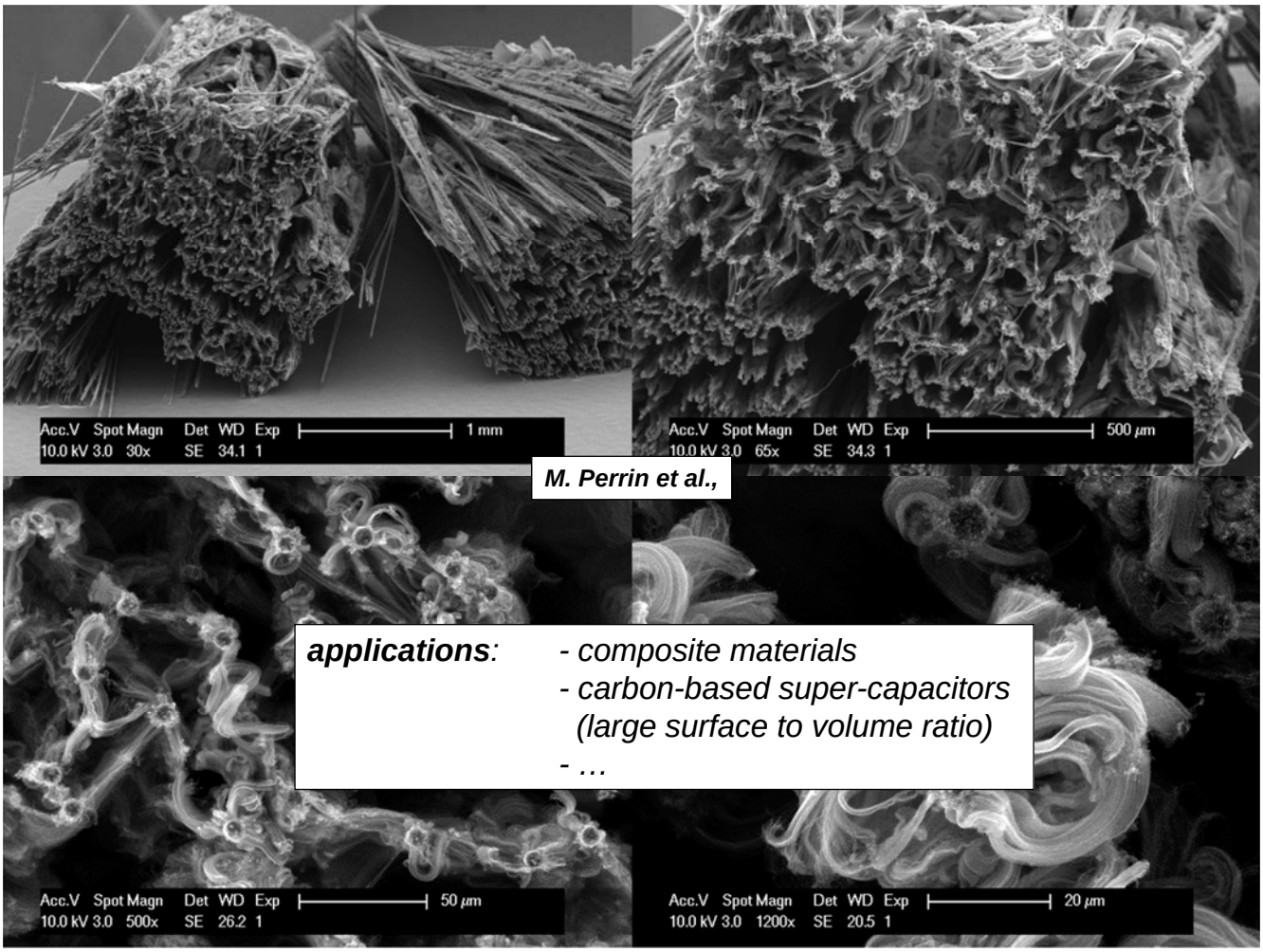
| | |
|---|---|
| hydrcarbon gases: | $C_2H_2$ (acetylene), $C_2H_4$ (ethylene), $CH_4$ (methane) (+ …) |
| carrier gases: | $H_2$, Ar |
| temperature: | 600-1000C |
| catalyst: | Fe (Ni, Co) |





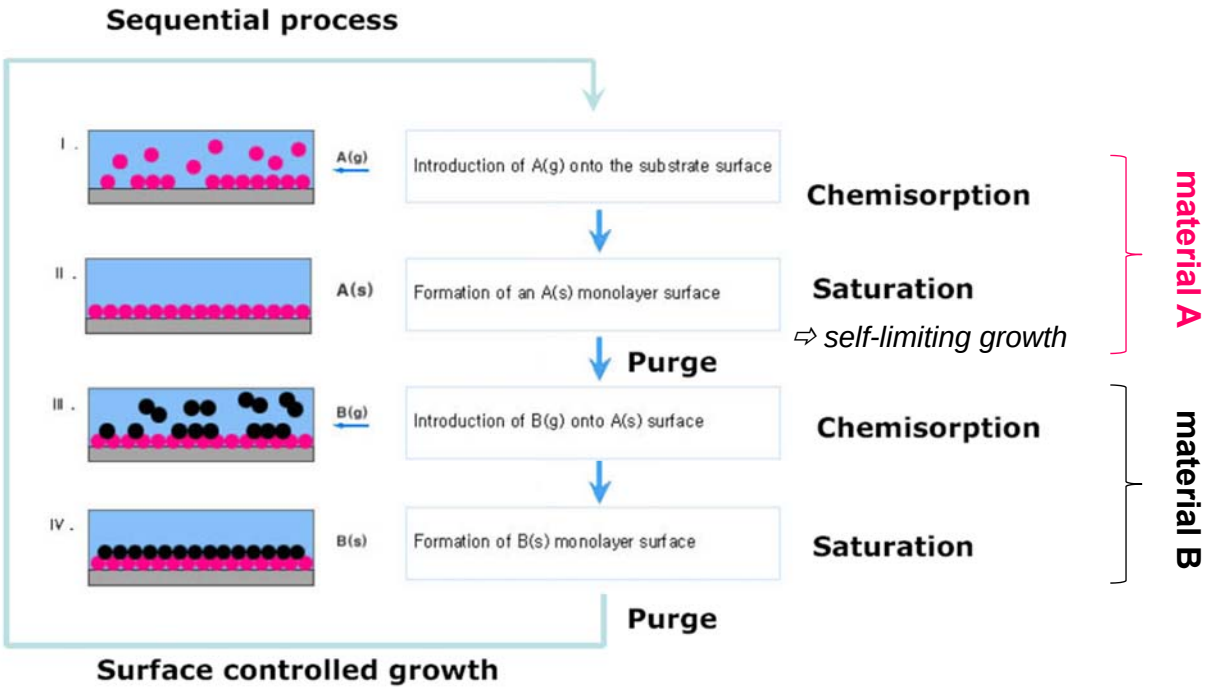

***M. Perrin et al.,***




***M. Perrin et al.,***

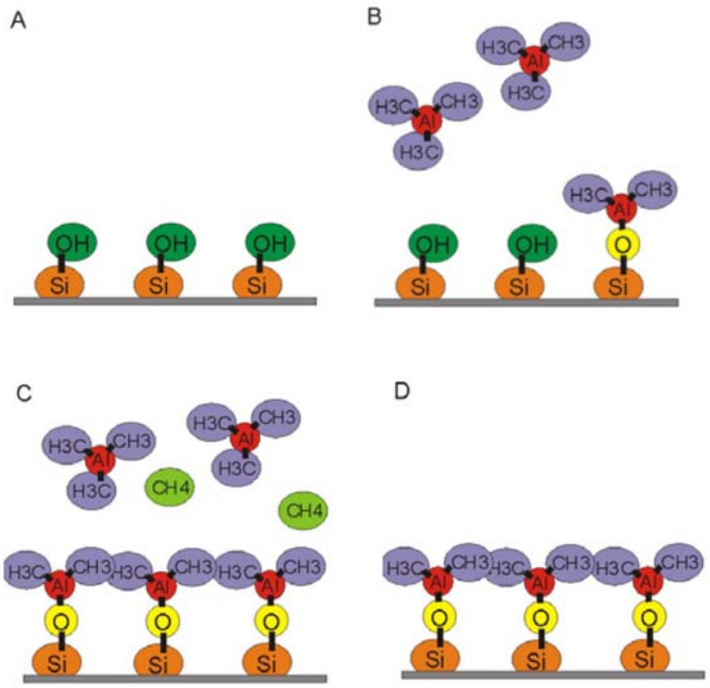
***applications**:*
- *composite materials*
- *carbon-based super-capacitors (large surface to volume ratio)*
- *…*

# Fabrication: Atomic Layer Deposition (ALD)



# Fabrication: Atomic Layer Deposition (ALD)

**example: deposition of $Al_2O_3$**




A: Hydroxylated surface

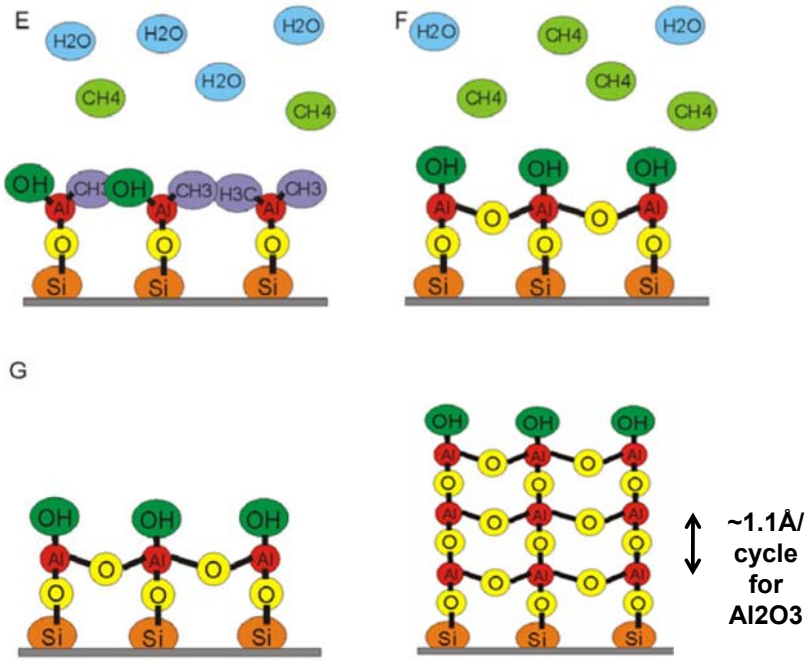
B: Trimethylaluminium (TMA) reacts with OH

C: TMA does not react with itself (passivation)

D: Purge reactor



# Fabrication: Atomic Layer Deposition (ALD)




E: $H_2O$ removes $CH_3$ and passivates

F: Purge reactor

G: Ready for new cycle

Repeat A-G for controlled monolayer deposition

# Fabrication: Atomic Layer Deposition (ALD)

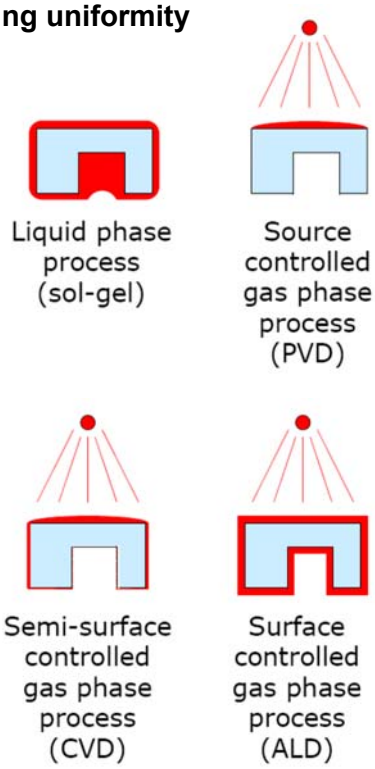
**typical conditions**

- Pressure 0.1-5 mbar
- Temperature 60-500ºC
- Gas flow 0.3-1.0 SLM (std liter / min.)

**variety of materials**

- Oxides (e.g. Al2O3, HfO2, TiO2, ZrO2 , Y2O3)
- Nitrides (e.g. AlN, TiN, WxN)
- Sulfides (e.g. ZnS, CaS)
- Fluorides (e.g. ZnF2, SrF2)
- Metals (e.g. Pt, Ir, Pd)
- Doped materials (e.g. ZnS:Mn, ZnO:Al)
- Polymers (polyimides)
- Biocompatible thin films (hydroxyapatite)

**Coating uniformity**






# Outline

- Introduction:
  overview, state of the art,
  semiconductor physics reminder

- Fabrication basics
  - IC fabrication overview
  - clean-rooms
  - Silicon: from sand to wafer
  - material deposition techniques (additive →)
  - etching (subtractive →)
  - lithography
  - examples of devices: MEMS, NEMS

- Outlook: new and future techniques

# Fabrication: etching

**Chemical**:

- wet etching (can be anisotropic due to crystal-face selectivity)
- *fast, up to 10μm/min or more*

**Physical etching** (sputtering)

- ion milling, FIB (focused ion beam)
- dry etching (plasma assisted techniques, pressures up to 10mbar)
  (more a combination of physical and chemical material removal)
- *slower, typ. 100Å -1000Å/min*

key points:

**selectivity** (etch rates ratio of masking layer and layer to etch)

**directionality** (defines etch profile)

note:

CMP, chemical mechanical polishing to achieve global planarization

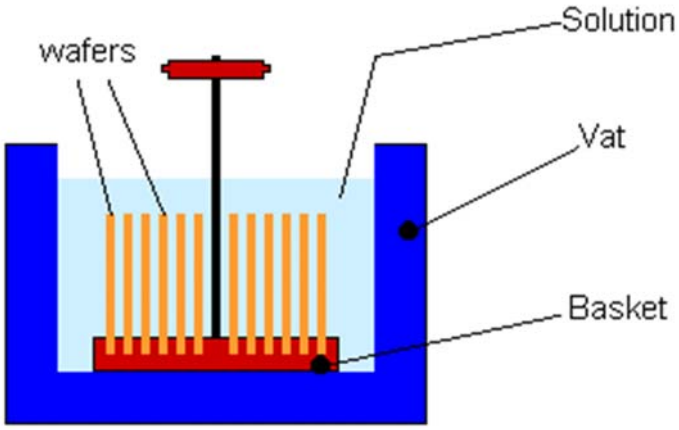
*combine mechanical abrasion with chemical etching; key parameters: force, slurry type, pad velocity*



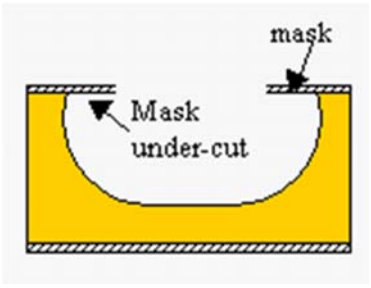
# Fabrication: wet etching

- **use chemical solutions to dissolve material**

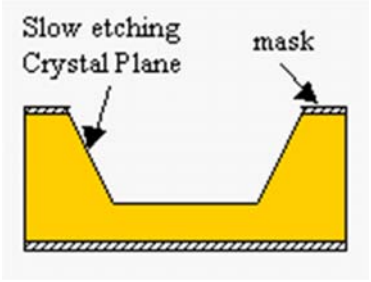
- chemical species react with surface
  ⇨ etch products ⇨ rinse, dry




isotropic, typ. 10μm/min




anisotropic, typ. 1μm/min






*http://www.memsguide.com*

# Fabrication: wet etching

**$SiO_2$** 6:1, buffered in $NH_4F$ (**BHF**) or 10:1 to 100:1 (by vol.) **HF** in $H_2O$
*NB: 1:1 HF (49% HF in $H_2O$) too fast*

$SiO_2 + 6\ HF \rightarrow H_2SiF_6 + 2\ H_2O$ ($H_2SiF_6$ soluble in $H_2O$)

**BHF** etch rate: **1000Å/min** (room temperature)
masks: photoresist, silicon nitride

***!! HF is extremely agressive: use adequate protection gear !!***

**Si** polycrystalline or single-crystal

isotropic: mix of $HNO_3$ and HF
(cyclic process: $HNO_3$ oxidizes Si, HF removes oxide)

$Si + HNO_3 + 6\ HF \rightarrow H_2SiF_6 + HNO_2 + H_2O + H_2$



# Fabrication: wet etching

**Si** anisotropic (cystalline Si): (100) rate / (111) rate ~ 100 at 80°C

e.g.: KOH
23.4% wt, $C_3H_8O$ 13.3% wt (isopropyl alcohol), $H_2O$ 63.3% wt

$Si + 4\ OH^- \rightarrow Si(OH)_4 + 4\ e^-$

exposes **slow planes** (111)
(~not attacked by etchant)

⇨V-shaped (or trapezoidal) groove for (100) wafers

⇨ vertical trench for (110) wafers

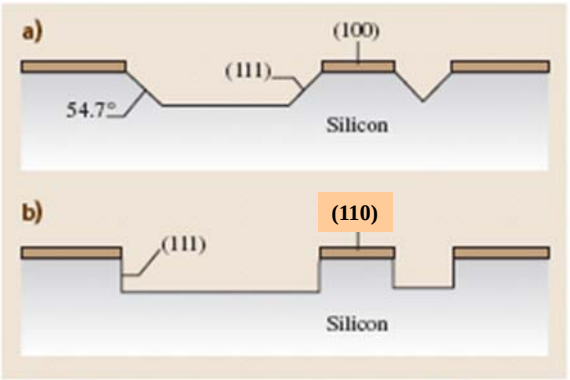
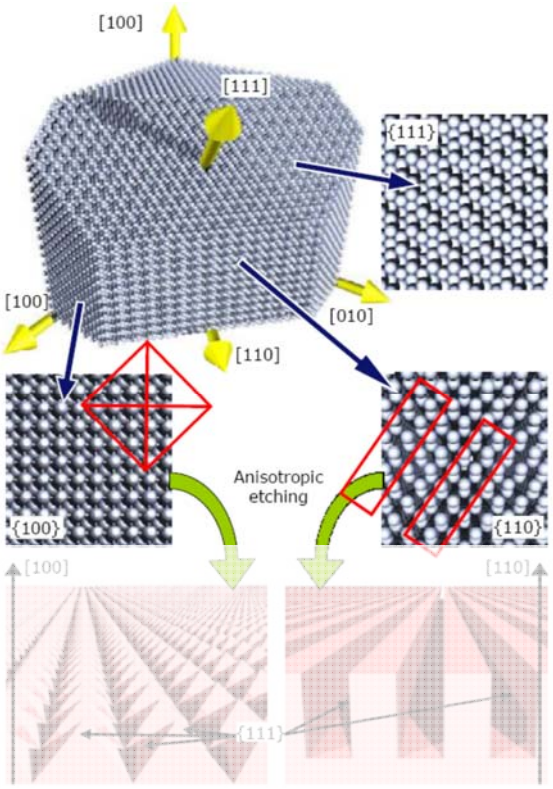



**Fig. 5.12a,b** Anisotropic etch profiles for: (a) (100) and (b) (110) silicon wafers

# Fabrication: wet etching






# Fabrication: wet etching

**$Si_3N_4$** $H_3PO_4$ 91.5% concentration at 180°C (etch rate ~ 100Å/min)

$Si_3N_4 + 4\ H_3PO_4 \rightarrow Si_3(PO_4)_4 + 4\ NH_3$

silicon phosphate ($Si_3(PO_4)_4$) and amonia ($NH_3$) are water soluble

selectivity to

| | |
|---|---|
| thermally grown $SiO_2$ | > 10:1 |
| Si | > 33:1 |

**metals**

| | |
|---|---|
| Al | mix of acids (phosphoric, acetic, nitric) and water |
| Ti | mix of sulfuric acid and hydrogen peroxide |

**NB**: **selectivity** ⇨ multilayers including stop layer for etching: well-defined wells

# Fabrication: dry etching

**dry etching**: usually plasma based

as compared to wet etch:

- smaller undercut (patterning of smaller lines)
- higher anisotropicity (high aspect-ratio structures possible)
- less selective
- mask etching not negligible

**ion milling**

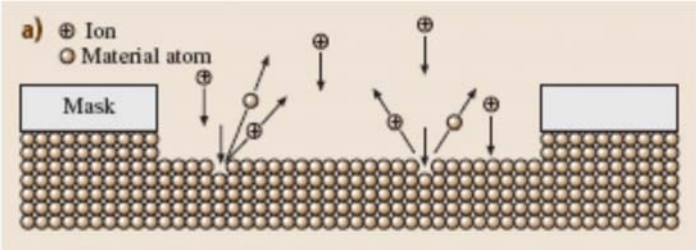
purely physical

sputering by accelerated $Ar^+$ ions

$p \sim 10^{-4} – 10^{-3}$ torr;

etch rate: few nm/min

note: no selectivity



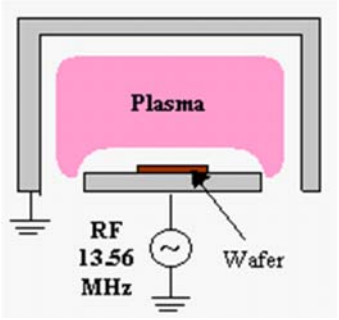



# Fabrication: dry etching

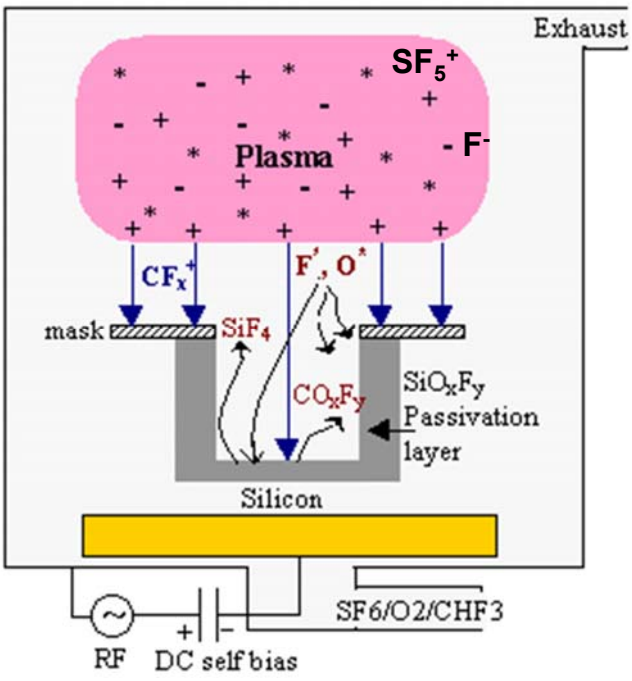
RIE: reactive ion etching

**physical and chemical**

- accelerated ions (e.g.: $Ar^+$, directional) either modify surface state (e.g.: bond breaking, makes surface more reactive) or help etch products to desorb
- reactive species (e.g. plasma generated from from SF6) diffuse to substrate surface and react, forming SiF4 (volatile)




**Si etch with $SF_6$**



# Fabrication: dry etching

DRIE (key process for MEMS)
**deep reactive ion etching**
*depth: up to few 100$\mu$m*

➔ ICP RIE

$SF_6$ alternated with $C_4F_8$ (to passivate walls), Bosch process

**selectivity**
**Si:SiO2, 150:1**
profile angle +/- 1°



*http://www.memsguide.com*

# Fabrication: dry etching

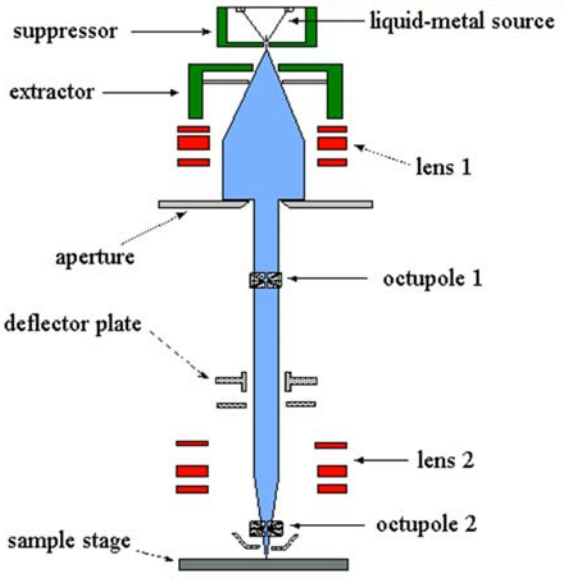
**SEM/FIB (FEI Nova 600 nanoLab)**

## Focused Ion Beam (FIB)

- controlled, directed heavy ion beam (typ. Ga)
- local ion milling (sputtering)
- fine structures, nm range

**Electrons**
- High penetration depth
- Low mass -> higher speed for given energy
- Electrons are negative
- Magnetic lens (Lorentz force)

**Ions**
- High interaction probability, less penetration depth
- Ions can remain trapped -> doping
- High mass -> slow speed but high momentum milling !!!
- Ions are positive
- Electrostatic lenses

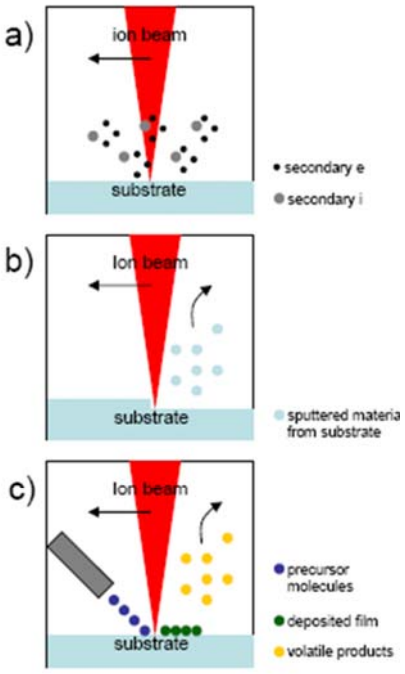



**IBM**

# Fabrication: dry etching

**FIB operating modes**

- Emission of secondary ions and electrons
  - FIB **imaging** ☛ a)
    low ion current
- Sputtering of substrate atoms
  - FIB **milling** ☛ b)
    high ion current
- Chemical interactions (gas assisted)
  - FIB **deposition**
  - Enhanced (preferrential) etching ☛ c)
- Other effects:
- Ion implantation
- Displacement of atoms in the solid
  - Induced damage
- Emission of phonons
  - Heating

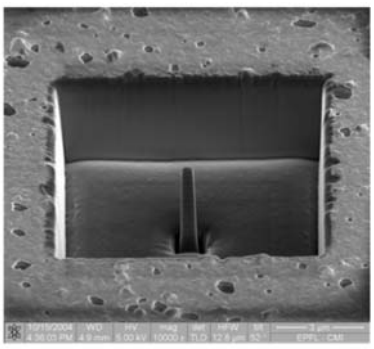




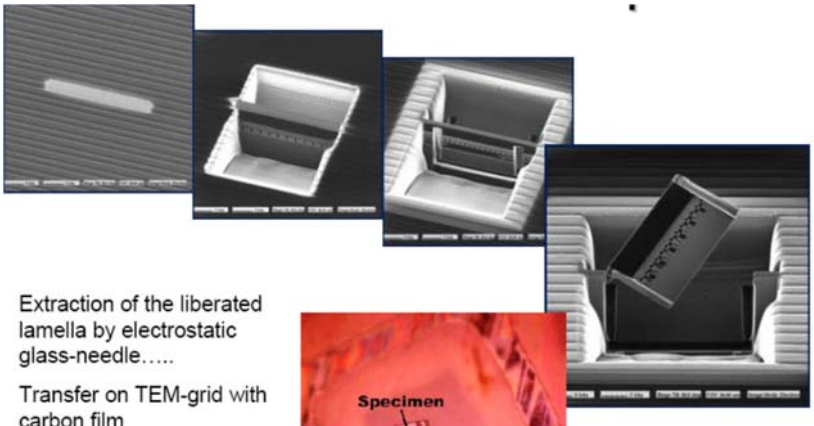

**Pavius et al., CMI EPFL**

# Fabrication: dry etching

**milling**

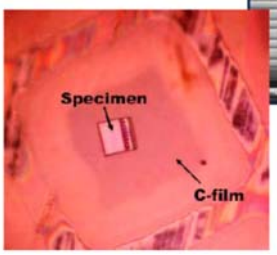


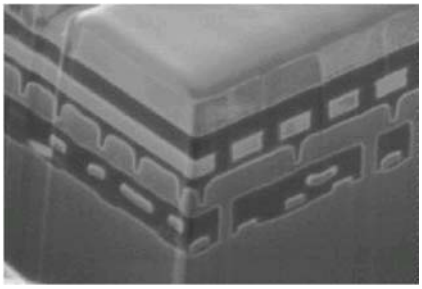
PZT-high aspect ratio „capacitor", W. Adachi (EPFL-LC)



Extraction of the liberated lamella by electrostatic glass-needle…..

Transfer on TEM-grid with carbon film



**local cross-sectioning of IC's (Uni Erlangen)**

## Fabrication: etching, short summary

Chemical:

- wet etching (can be anisotropic due to crystal-face selectivity)
- *formation of reaction products soluble in the etch solution or volatile at low pressures*

Physical etching (sputtering)

- ion milling, FIB (focused ion beam)
- dry etching (plasma assisted techniques, pressures up to 10mbar)
  (more a combination of physical and chemical material removal)
- *relies on momentum transfer of particles hitting and eroding the surface*

key points:

**selectivity** (etch rates ratio of masking layer and layer to etch)

**directionality** (defines etch profile)



## Outline

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  overview, state of the art,
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- Fabrication basics
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  - material deposition techniques
  - etching
  - lithography
  - examples of devices: MEMS, NEMS
- Outlook: new and future techniques

# lithography: Greek lithos "stone" + graphein "write"

**definition**: method to define a pattern on a substrate

typ.: pattern engraving on print block, inking and transfer to paper
(1st process, Senefelder, 1798)

• first synthetic photo-polymer: 1935, Eastman Kodak

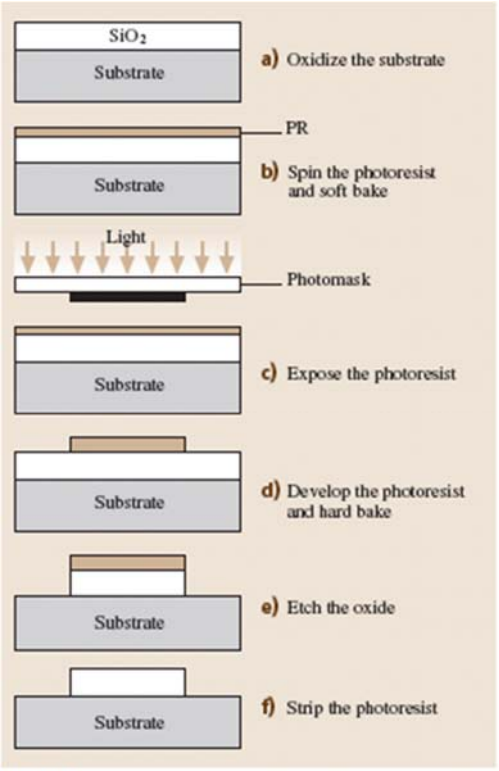



**Fig. 5.2** Schematic drawing of the photolithographic steps with a positive photoresist (PR)



# Optical lithography

## masking methods

**contact**
mask deteriorates

**proximity**
poorer resolution

**projection**
better resolution
(diffrac. limited)

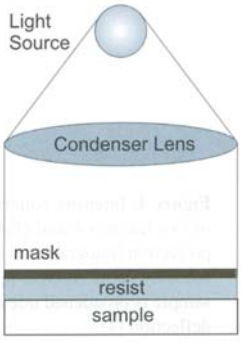
**Minimum Feature Size**

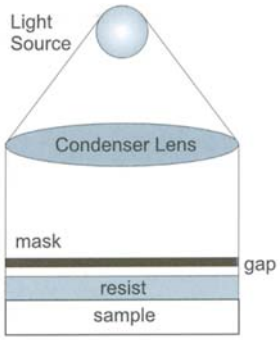
MFS ~ $(d\lambda)^{1/2}$

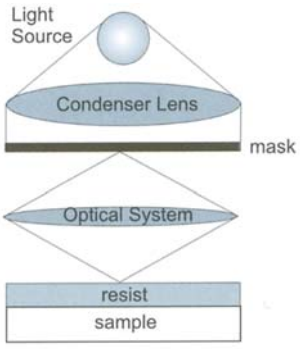
MFS ~ $[(d+g)\lambda]^{1/2}$

MFS ~ 0.61 $\lambda$/NA

*reduction possible (decreases errors), stepper (multiple exp.)*

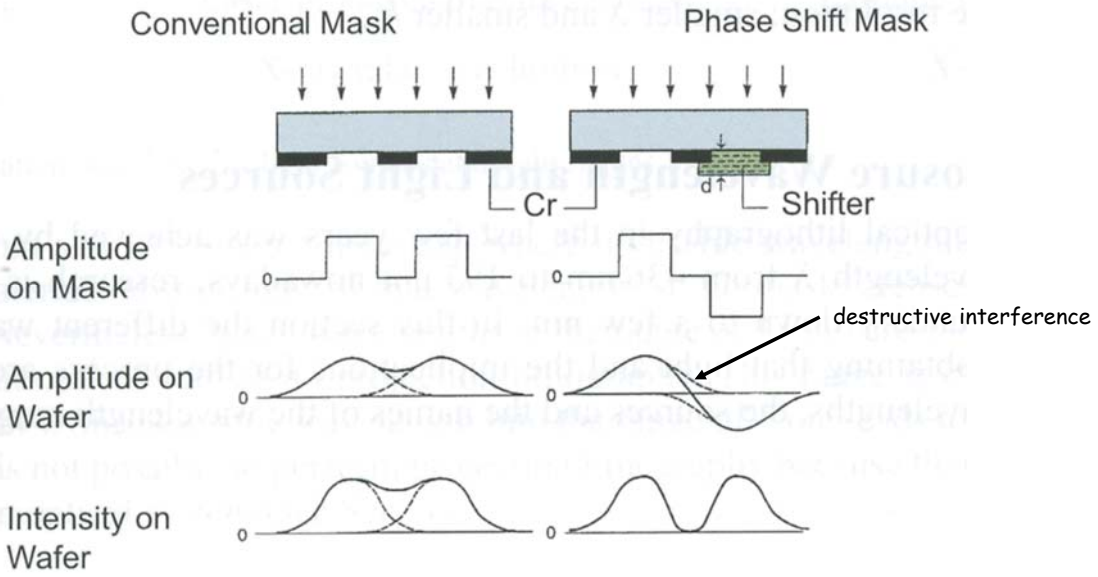


# Optical lithography

## phase-shifting technique






# Optical lithography

## photoresists profiles

(after development)

**R**: developing rate of exposed region

**R0**: developing rate of unexposed region

R/R0 > 10: fast developper

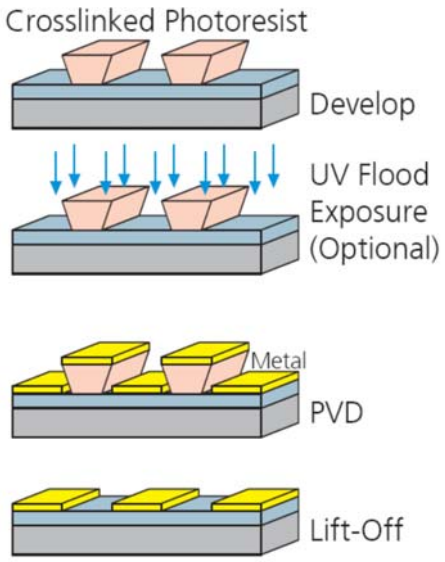
γ: resist contrast

(linked to exposure dose, cf Madou)

| Profile | Dose | Developer Influence | $R/R_0$ | γ | Uses |
|---|---|---|---|---|---|
| A.Positive resists Undercut a) 95-110° | High ( often with back scatter radiation) | Low | > 10 | > 6 | Ion implant, lift-off Not good for plasma etching. Often only obtained through image reversal |
| Vertical b) 75-95° | Normal dose | Moderate | 5 - 10 | < 4 | Lift-off, Reactive ion etch wet etch Ion beam etch Perfect fidelity |
| Normal or overcut c) 45-75° | Low | Dominant | < 5 | < 3 | Typical for positive resists, wet etch, metallization < 20% resist loss |

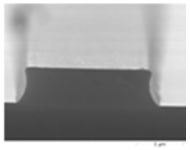
# Optical lithography

**Example: lift-off process, undercut control**
ma-N 400 negative resist (micro resist technology), **2 µm** thickness

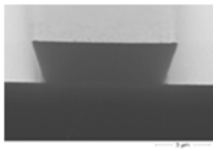



**Effect of exposure time**

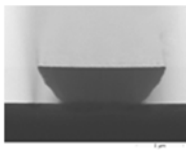
$t_E$ 90 s,
0 µm undercut



$t_E$ 100 s,
0,5 µm undercut



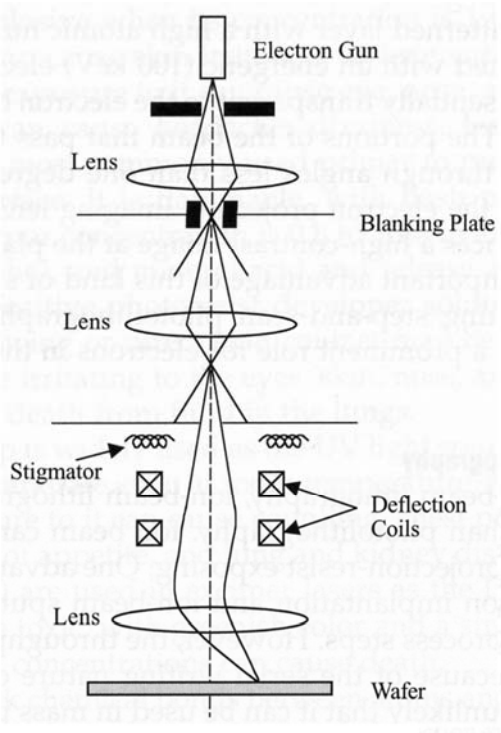
$t_E$ 140 s,
1,5 µm undercut





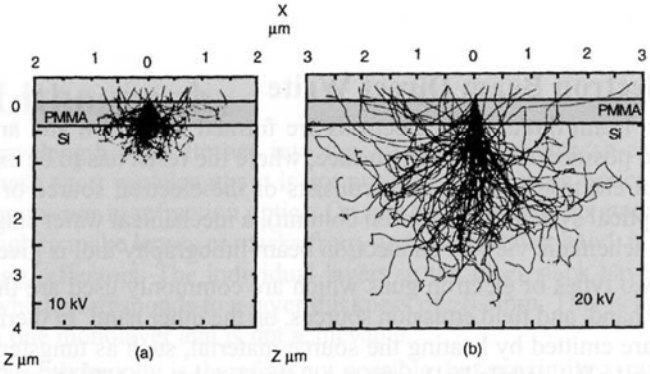
***micro resist technology***

# electron beam lithography (EBL)




precise (energy, dose)
relatively slow
(industrial application: parallel beams)
resolution limit ~ 10nm (50nm)
no mask
large DOF

large scattering of electrons

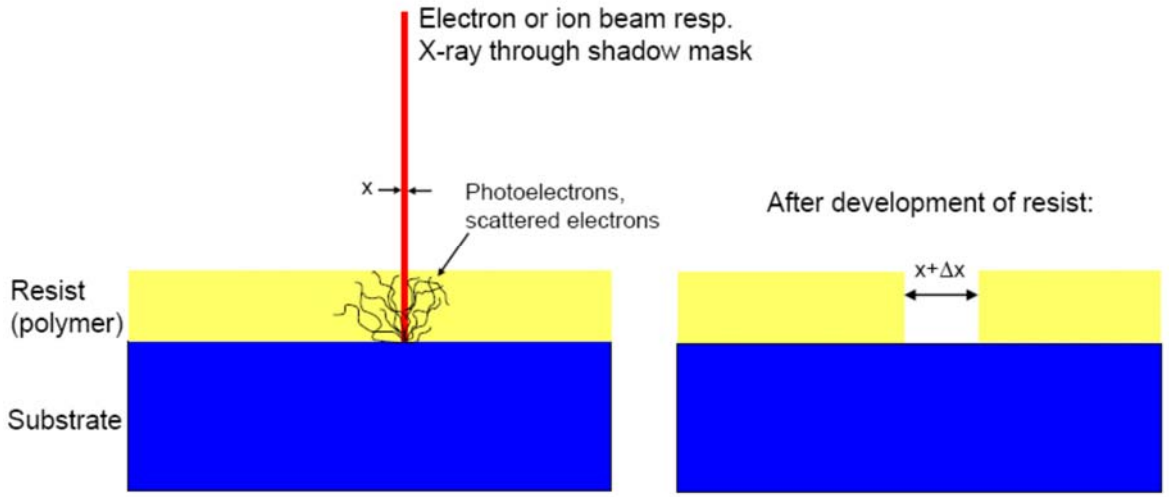





*Refs. 1 & 3*

# electron beam lithography (EBL)

proximity effects



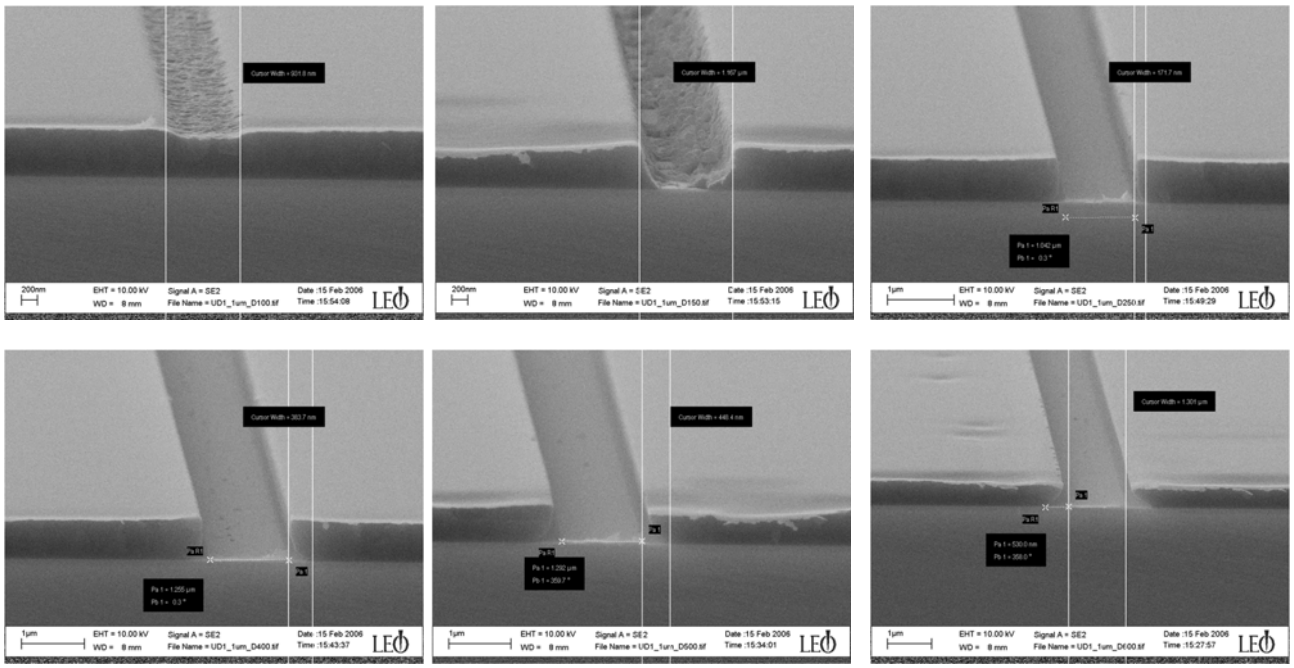



*J. Gobrecht, PSI*

# electron beam lithography (EBL)

dose test on PMMA: overcut to **undercut** (A. Kleine)

note: undercut
critical for lift-off



# electron beam lithography (EBL)

**EBL compared to optical/UV lithography**

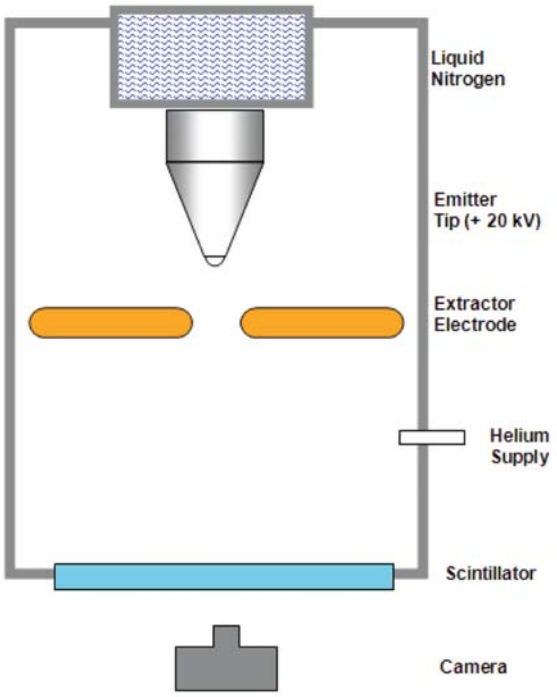
+ precise control of dose delivery
+ fast beam deflection and modulation
+ smaller spot on resist (<10nm) as compared to light (500nm), increased resolution
+ no mask needed (direct writing, "software" mask)
+ large depth of focus

- strong electron scattering in solids (practical resolution > 10nm)
- operation in vacuum (electron beam)
- slow exposure speed (scanning)
- high cost



# A recent new tool for lithography: He ion microscope

**He microscope**



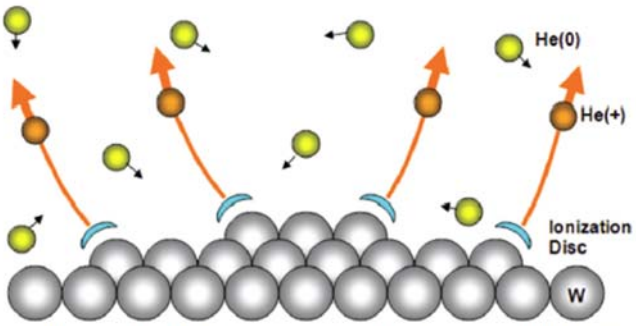




*Figure 2: Neutral helium atoms (yellow) are drawn towards the tip by a polarization effect. When they pass through the ionization disk (blue) they are ionized (orange) and are accelerated away from the tip.*



***Morgan et al., Microscopy Today 2006***

# Fabrication: dry etching

## Helium ion microscope

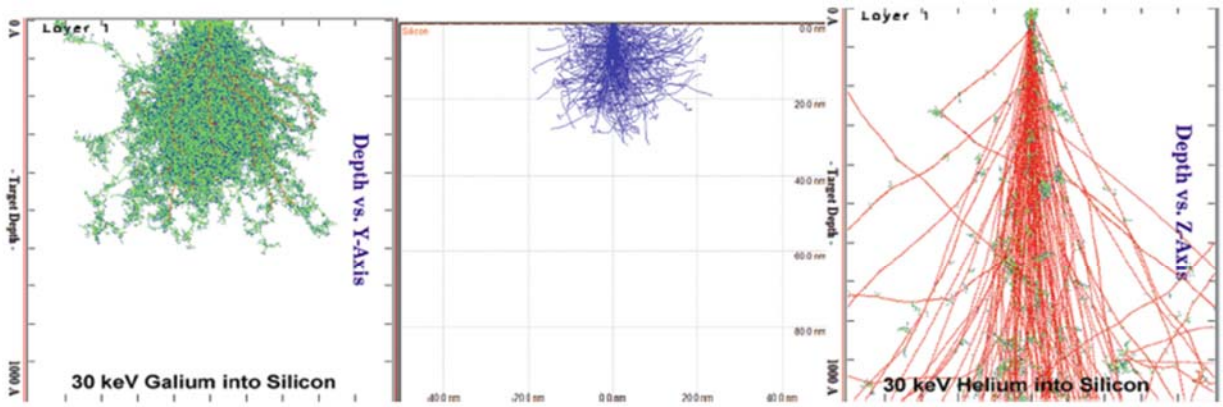



*Figure 7: Interaction volume of 30keV Gallium (left), 1 keV SEM (center), 30keV Helium (right).*

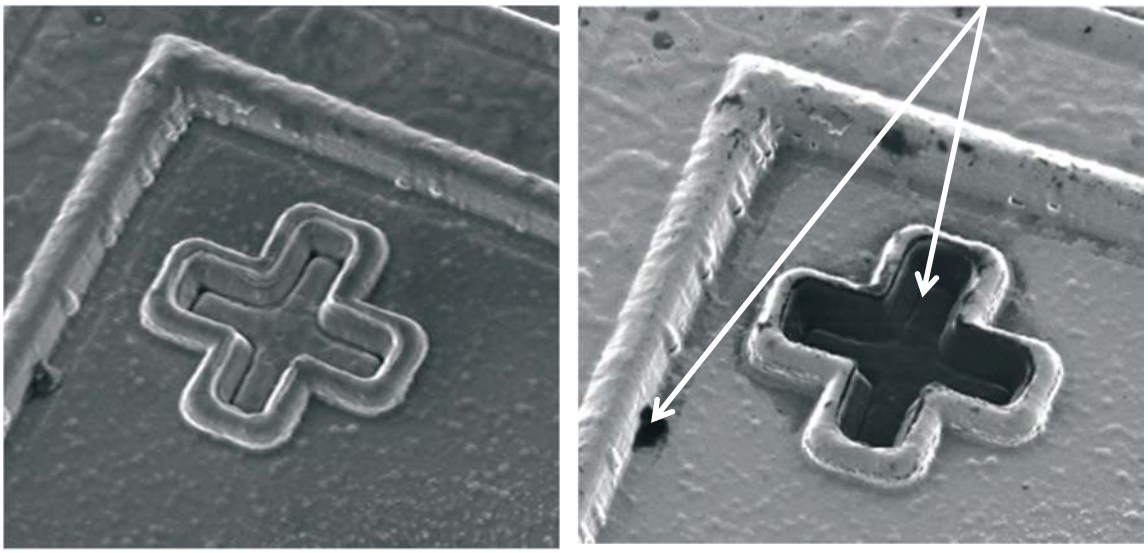


*Morgan et al., Microscopy Today 2006*

# Fabrication: dry etching

## Helium ion microscope: imaging & contrast

***different material***



**SEM image (secondary electrons)**

**HE ion image: more secondary electrons emitted (2-8) per ion and material dependent**



*Morgan et al., Microscopy Today 2006*

# Fabrication: dry etching

**Helium ion microscope: lithography**

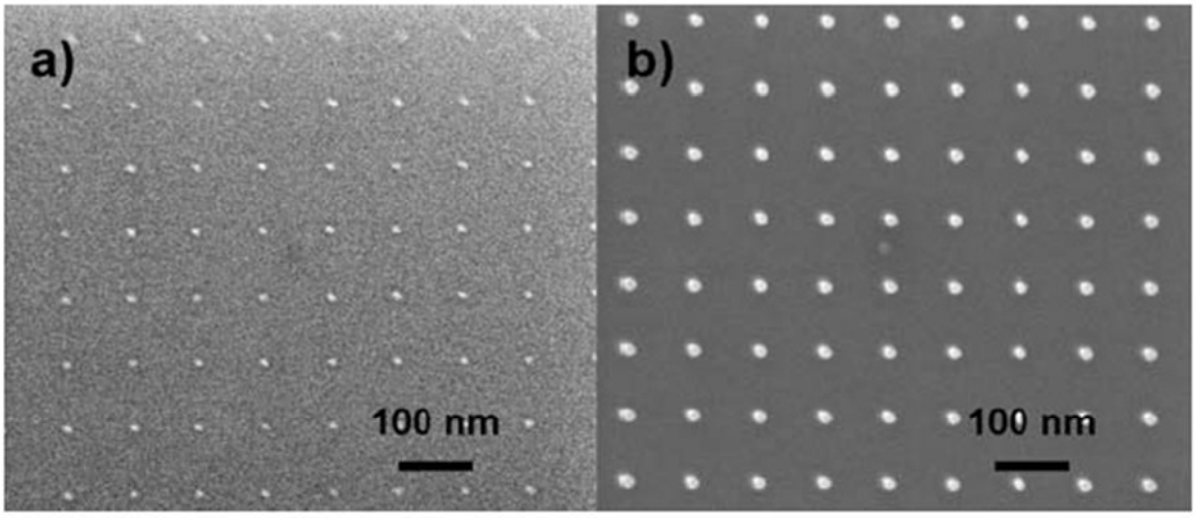



*Figure 3. Dot exposures in HSQ.*
*Left: 5 nm thick resist. Right: 55 nm thick resist.*

**~14nm dots**

**~6nm dots**



# Fabrication: dry etching

**Helium ion microscope: milling of nano-ribbons in suspended graphene**

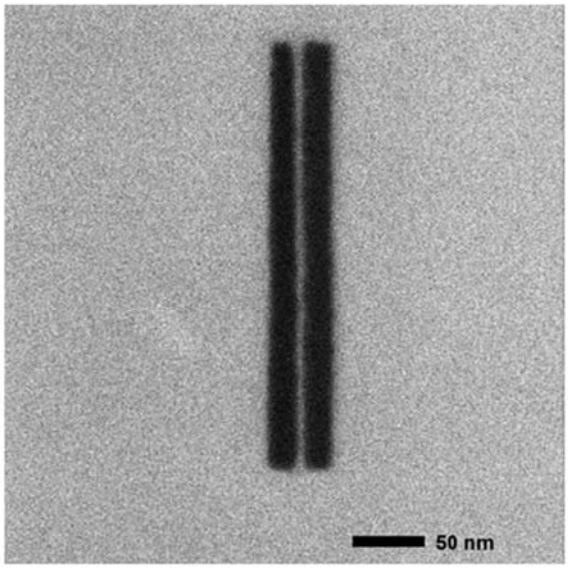



*Figure 4. A 5 nm wide ribbon machined in suspended graphene with a 60:1 aspect ratio.*

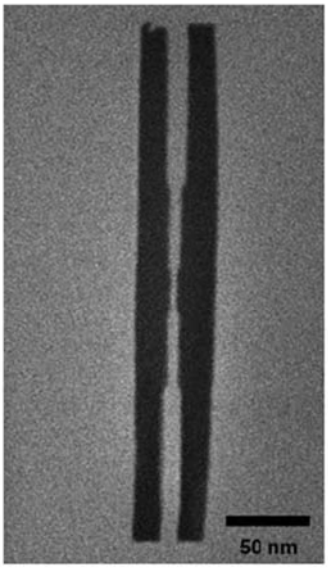



*Figure 5. A nano-ribbon machined to have stepped width.*

# Outline

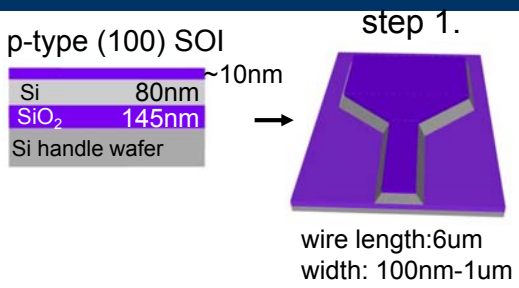
- Introduction:
  overview, state of the art,
  semiconductor physics reminder

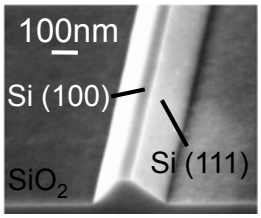
- Fabrication basics
  - IC fabrication overview
  - clean-rooms
  - Silicon: from powder to wafer
  - material deposition techniques
  - etching
  - lithography
  - examples of devices

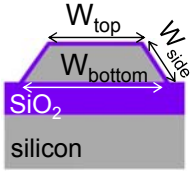


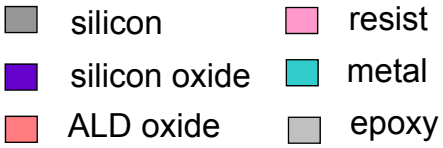
# SiNW-ISFET Fabrication

1. sensor etching
2. contact implantation
3. gate oxide deposition
4. contact metallization
5. packaging
6. surface functionalization
7. microfluidic system




*K. Bedner, A. Tarasov, M. Wipf, R. Stoop et al.*

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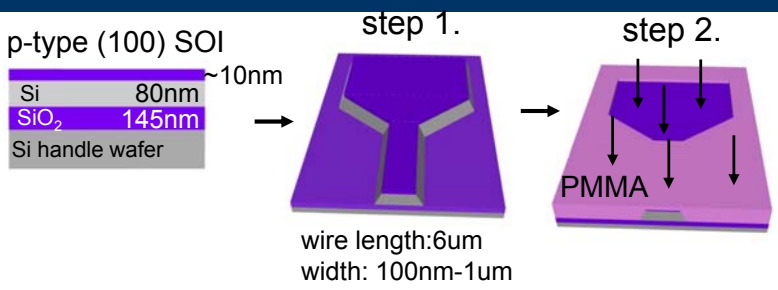


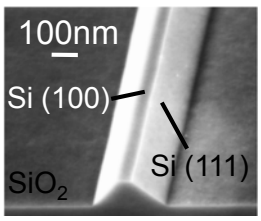


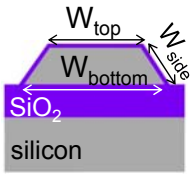


silicon
silicon oxide
ALD oxide
resist
metal
epoxy

*K. Bedner, A. Tarasov, M. Wipf, R. Stoop et al.*


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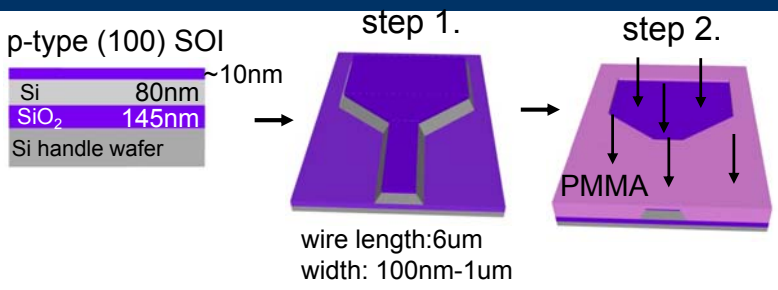


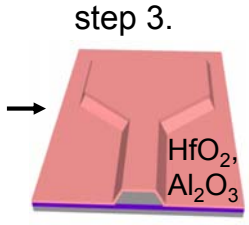


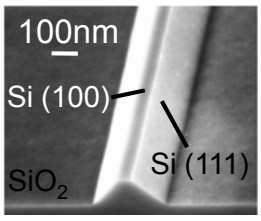


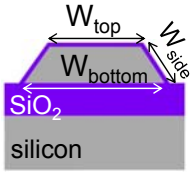



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*K. Bedner, A. Tarasov, M. Wipf, R. Stoop et al.*

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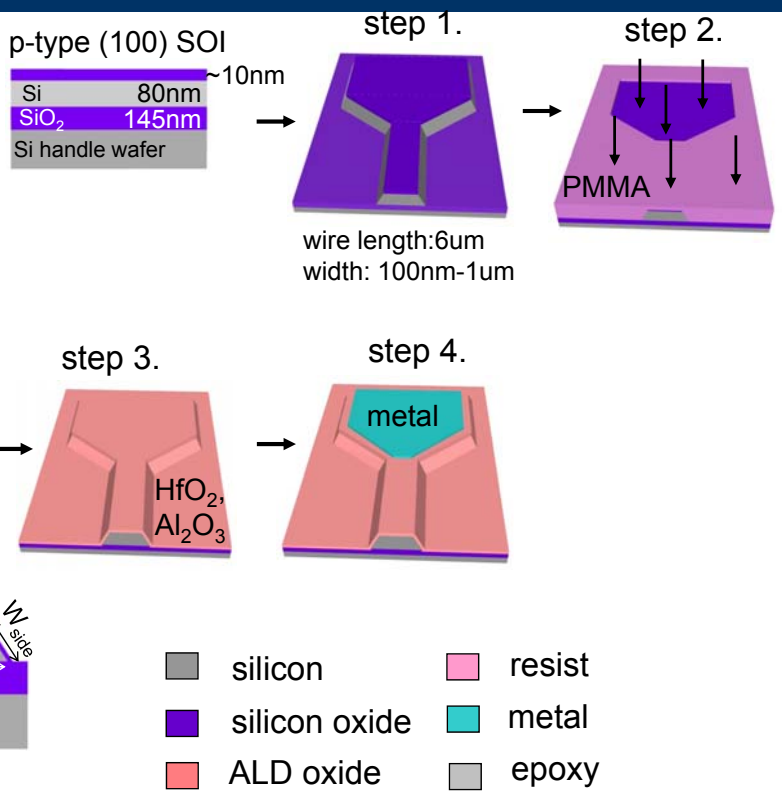


*K. Bedner, A. Tarasov, M. Wipf, R. Stoop et al.*


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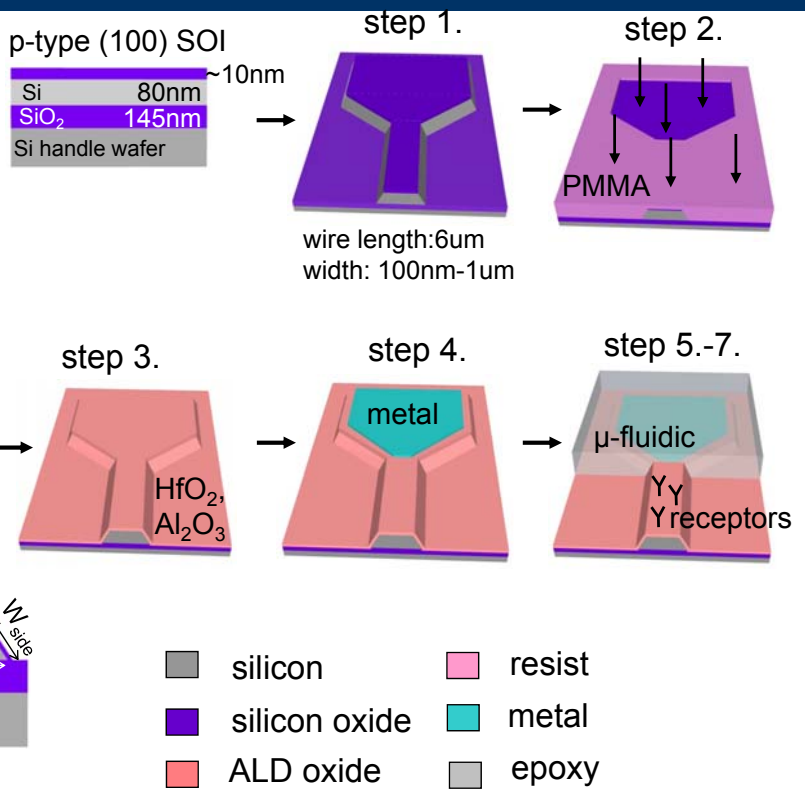
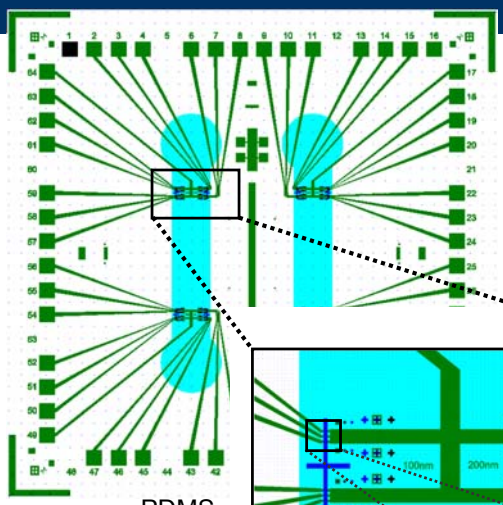




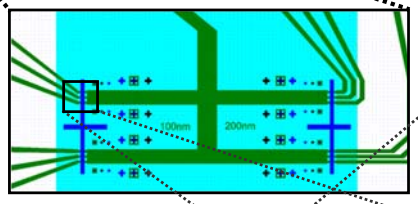
*K. Bedner, A. Tarasov, M. Wipf, R. Stoop et al.*

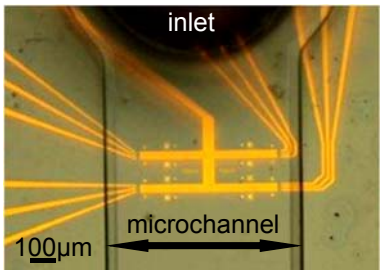
# SiNW-ISFET Fabrication

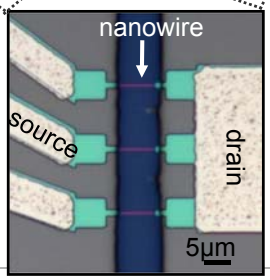
48 silicon nanowires/sample
**top width: 100nm – 1µm**

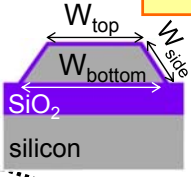


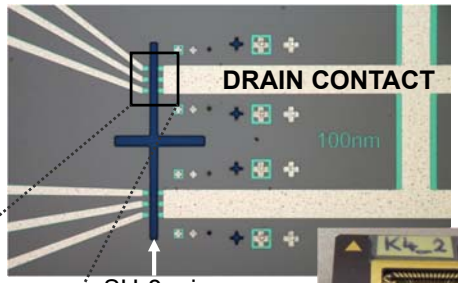
PDMS microfluidic



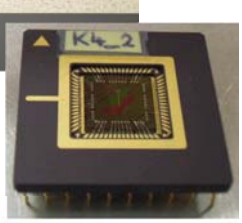


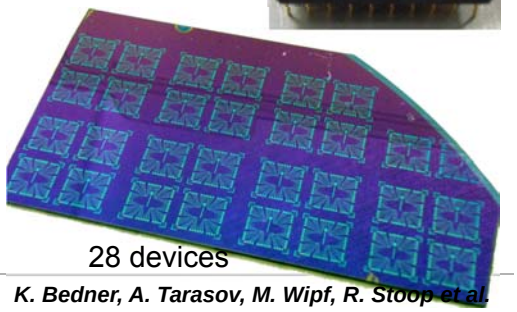




SU-8 micro-channel





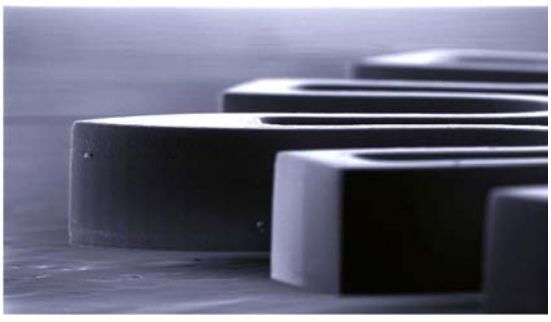
28 devices

*K. Bedner, A. Tarasov, M. Wipf, R. Stoop et al.*

# MEMS/NEMS and devices

from MEMS (micro-electromechanical systems) …

e.g. Si gears for watch industry: lower friction and inertia



# MEMS/NEMS and devices

## … down to NEMS

- masses in $10^{-15}$g to $10^{-18}$ g range ($\propto L^3$)
- resonators above 10GHz ($\propto 1/L$)
  (f ~ (spring cst/eff. mass)$^{1/2}$, spring constant $\propto$ L)
- very low power: $10^{-18}$W threshold (thermal fluc. at 300K)
- low dissipation, high Q factor: sensitive to damping ➔ sensors
  (sensitivity potentially reaching quantum limit)

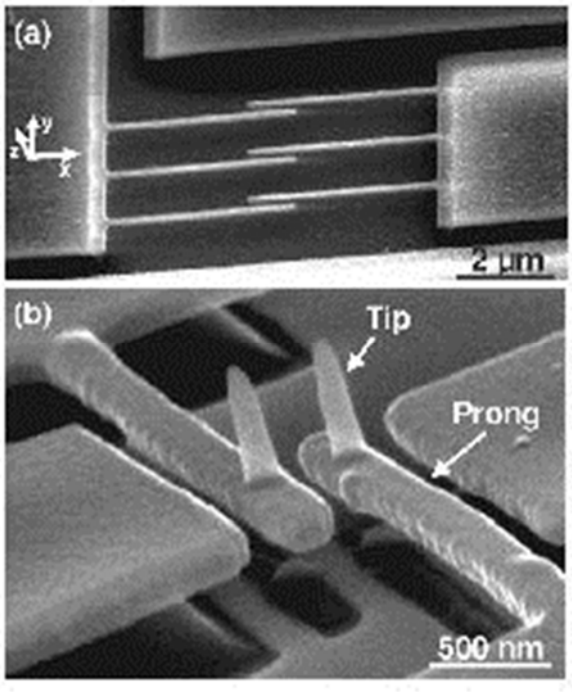
- NB: 10x10x100 nm Si beam contains ~ 5 x $10^5$ atoms,
  among which ~3 x $10^4$ reside at the surface
  (i.e.: > 10% of the constituents are **surface or near-surface atoms**)



# MEMS/NEMS and devices

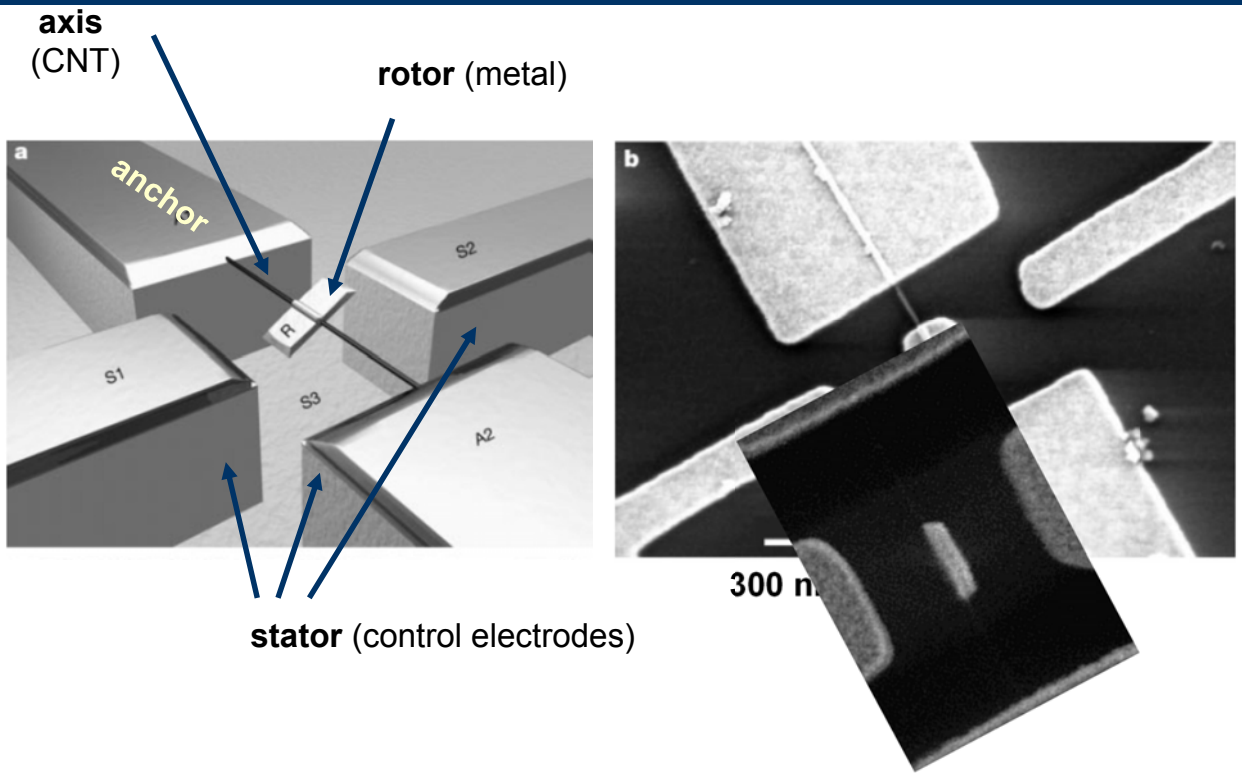
nano-tweezers:
electrostatic actuation

actuation amplitude
down to 6 pm (rms)/ sqrt(Hz)




Ch. Meyer, H. Lorenz, and K. Karrai, "Optical detection of quasi-static actuation of nanoelectromechanical systems" Appl. Phys. Lett. **83**, 2420 (2003).

# MEMS/NEMS and devices






*Fuhrer, Zettl et al., Nature 2004*

# Integration: hybrid devices

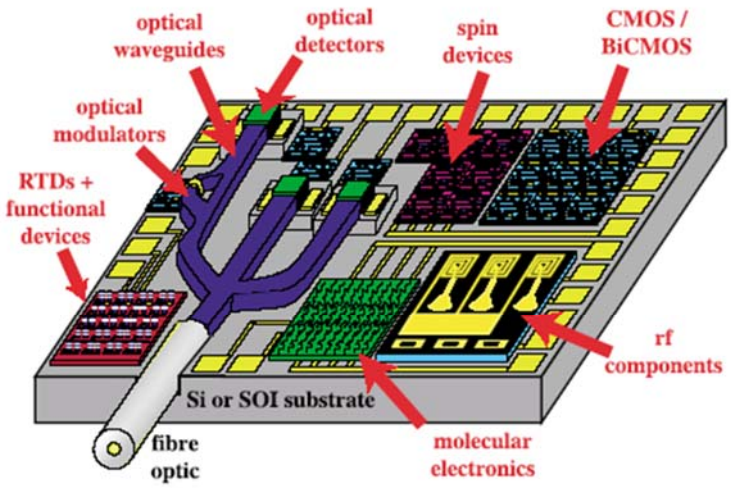
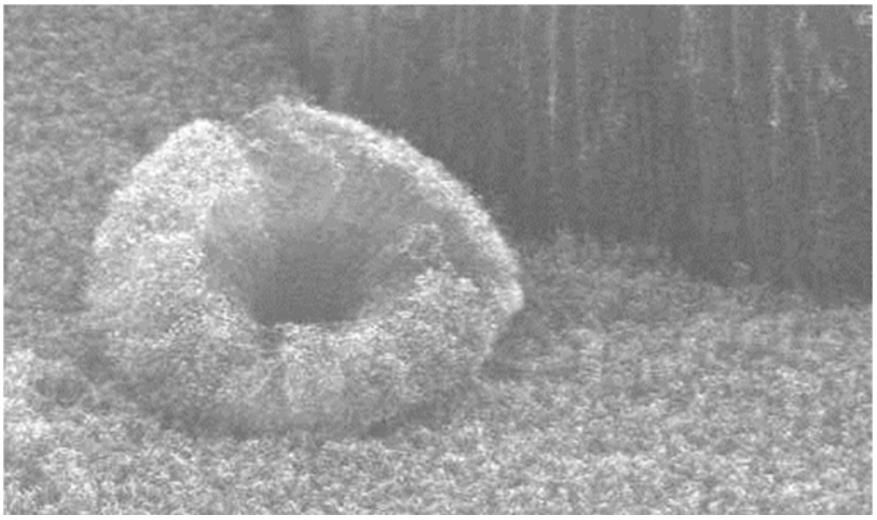



*Figure 4: the System-on-a-Chip of the Future?*

*Full compatibility of new technologies with CMOS is desirable, but a complete integration may be too expensive or suffer from severe technological drawbacks such as crosstalk or RF incompatibility. Multi-chip modules may therefore be a more adequate solution for specific applications.*



*Tech. Roadmap for Nanoelectronics, IST program, European Commission*





# Sources and ressources

**Books**

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- **Nanoelectronics and Information Technology**
  R. Waser ed., Wiley-VCH, 3rd edition, 2012

- **VLSI Technology** (more physical)
  SM. Sze, 2nd ed., McGraw-Hill, 1988

- **Introduction to Semiconductor Manufacturing Technology**
  H. Xiao, Prentice-Hall, 2001.